

PCB Number: 10086-1M

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55	ATI Mad_MEMORY	
56	ATI DDR3 64MX16_A	
57	ATI DDR3 64MX16_B	
58	ATI THERM & STRAPS	
59	GPU_ISL_IN GFX_VCORE	
60	GPU RT8015 VGA 1.0/1.8V	
61	DISPLAY PORT SWITCH	
62	VGA IN	

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PCB BOARD SIZE  
244mmX 244mm  
4 Layer

Internal Slot/Header  
Front/Rear IO  
Chipset

VRM 12  
(3 Phase 65W)

DDR3 SO-DIMM

DDR3 SO-DIMM

INTEL  
Sandy Bridge  
SOCKET FCLGA LGA1155  
(65W)  
0.9144mmX0.9144mm

Clarksfield option external GPU

AMD  
Whistler/  
Seymour

HDMI\_OUT

TMD5

MUX\_B\_I

MUX\_A\_I

Channel A  
64 bit  
1066/1333MHZ

Channel B  
64 bit  
1066/1333MHZ

100MHz

PCI-E x16 BUS

PECI 3.0

FDI

DMI

PECI

HDMI

MUX\_B\_I

HDMI

D-SUB PORT  
Debug Header

RGB

MUX\_A\_I

LVDS

SCALAR  
RTD2281W

DVI

USB2.0X2 SIDE

USB 2.0 \*9

480Mb/s

USB 2.0 x4 REAR

SPI Flash ROM  
16M

SPI BUS

WEBCAM \ Touch  
\ Card Reader

SATA \*1  
Slim ODD

SATA2.0 BUS

SATA \*1  
3.5" HDD

SATA2.0 BUS

SIDE  
Speaker

SIDE  
MIC -IN

SIDE  
HP - OUT

HDA CODEC  
ALC269Q

High Definition Audio

INTEL PCH  
Sugar Bay

FCBGA 989PIN  
?X?mm

MINI PCI-E  
WLAN

PCI-E Gen1 Interface

MINI PCI-E  
SSD

SATA 2.0

LAN  
82579ML

PCI-E Gen1 Interface

RJ45

25M

120MHz  
100MHz  
96MHz  
48MHz  
33MHz  
14.318MHz  
32.768KHz

32.7K

SIO NCT6681D

CPU 1X4 FAN

PSU 1X4 FAN

SYS 1X4 FAN

14.318MHz  
33MHz  
24MHz or 48MHz  
96MHz  
100 MHz  
120 MHz  
PCH  
CLOCK  
Buffer  
Page 20

12PIN PWR CONN  
12V & 5VSB

25M

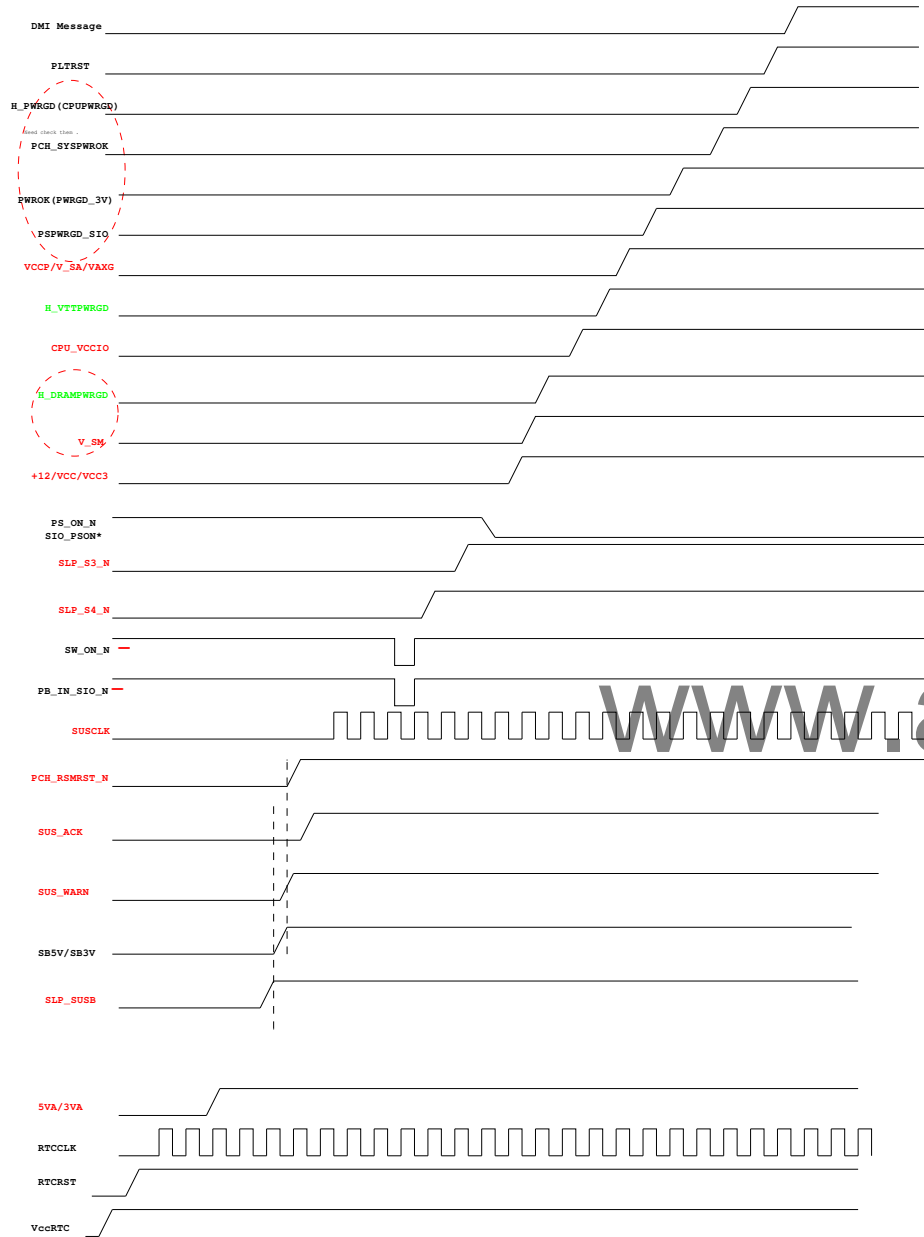
wistron

Wistron Incorporated  
12F, 88, Hsin Tai Wu Rd  
Hsinchu, Taipei

Title  
Size C Document Number  
Tahoe  
Date: Wednesday, March 30, 2011 Sheet 2 of 62

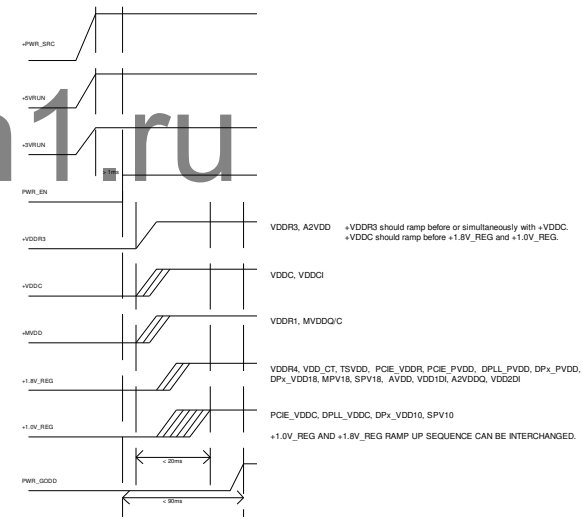


# POWER ON SEQUENCE

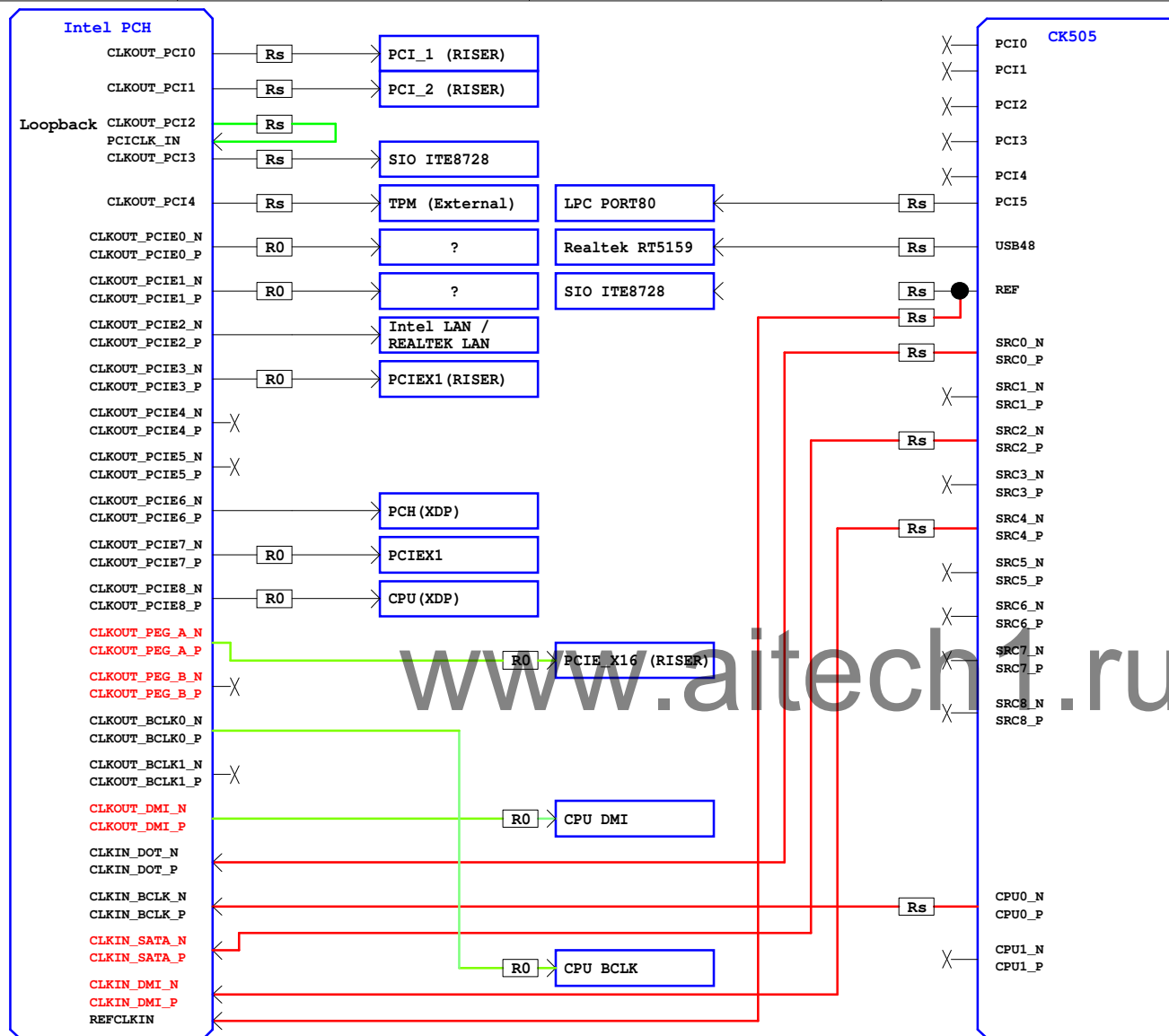


## GPU CEDAR POWER SEQUENCE

### POWER UP SEQUENCE (Not to scale)







BTM: Buffer Through Mode  
Need CK505 to provide 4 clock to PCH

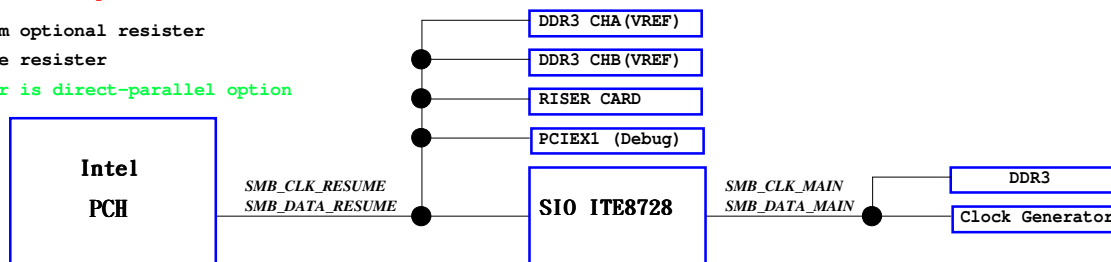
FCIM: Full Clock Intergration Mode  
Remove CK505

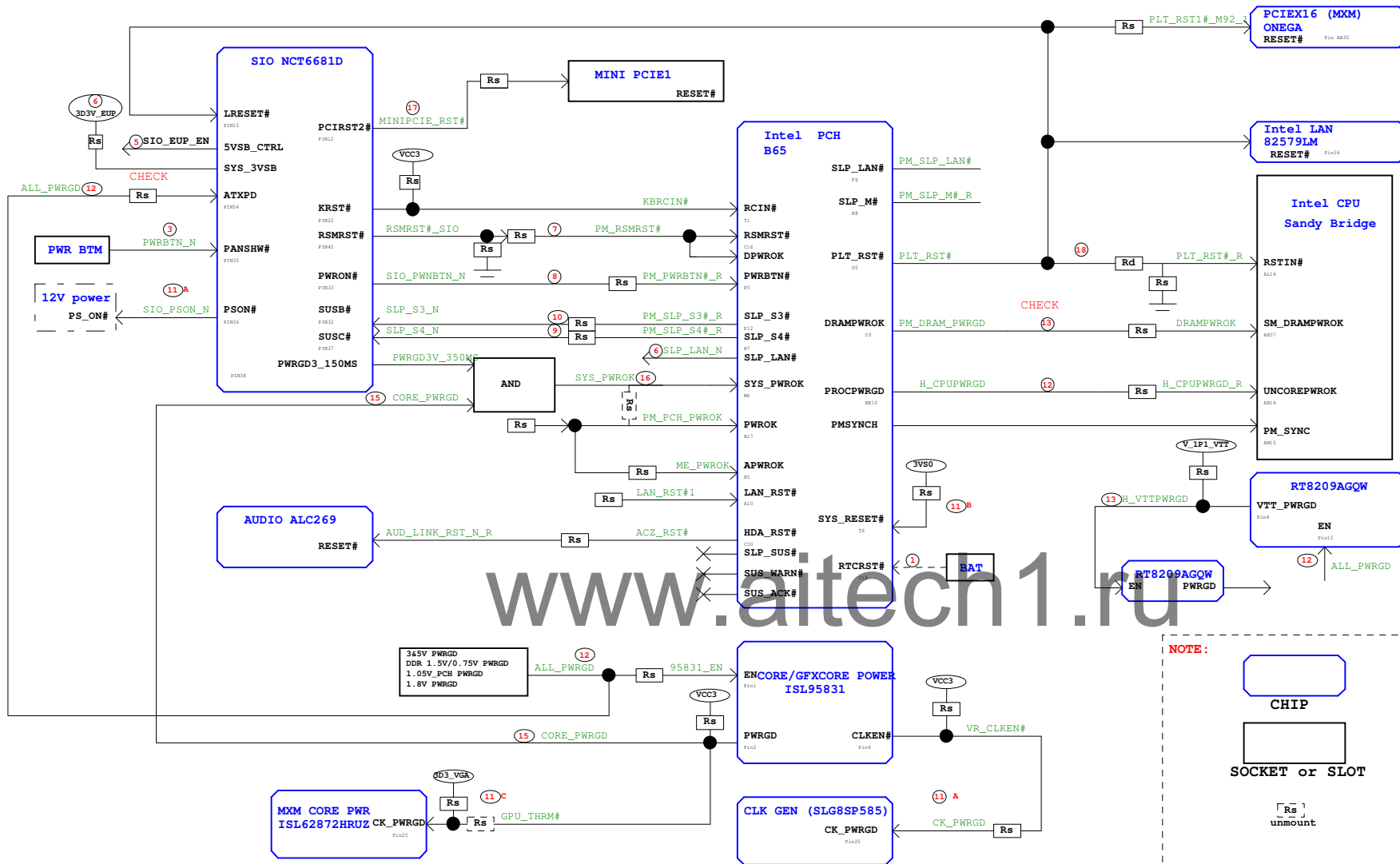
Note: Red Color is Gen2 spec.

Note: R0 is 0 ohm optional resistor

Note: Rs is serie resistor

Note: Green Color is direct-parallel option






**NOTE:**

CHIP

SOCKET or SLOT

[Rs] unmount

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		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title CLOCK GEN			
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		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title RESERVE			
Size C	Document Number Tahoe		Rev SA
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## DDR DATA

15 M\_DATA\_A[0..63] <<>  
16 M\_DATA\_B[0..63] <<>  
15 M\_DQS\_A\_DP[0..7] <<>  
15 M\_DQS\_A\_DN[0..7] <<>  
16 M\_DQS\_B\_DP[0..7] <<>  
16 M\_DQS\_B\_DN[0..7] <<>

## DDR CMD/ADD

15 M\_MAA\_A[0..15] <<>  
16 M\_MAA\_B[0..15] <<>  
15 M\_WE\_A\_N <<>  
15 M\_CAS\_A\_N <<>  
15 M\_RAS\_A\_N <<>  
15 M\_SBS\_A0 <<>  
15 M\_SBS\_A1 <<>  
15 M\_SBS\_A2 <<>  
16 M\_WE\_B\_N <<>  
16 M\_CAS\_B\_N <<>  
16 M\_RAS\_B\_N <<>  
16 M\_SBS\_B0 <<>  
16 M\_SBS\_B1 <<>  
16 M\_SBS\_B2 <<>

## DDR CTRL

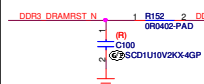
15 M\_SCS\_A\_N0 <<>  
15 M\_SCS\_A\_N1 <<>  
15 M\_SKE\_A0 <<>  
15 M\_SKE\_A1 <<>  
15 M\_ODT\_A0 <<>  
15 M\_ODT\_A1 <<>

## DDR CLOCK

15 CK\_M\_DDR0\_A\_DP <<>  
15 CK\_M\_DDR0\_A\_DN <<>  
15 CK\_M\_DDR1\_A\_DP <<>  
15 CK\_M\_DDR1\_A\_DN <<>  
16 CK\_M\_DDR0\_B\_DP <<>  
16 CK\_M\_DDR0\_B\_DN <<>  
16 CK\_M\_DDR1\_B\_DP <<>  
16 CK\_M\_DDR1\_B\_DN <<>

## DDR OTHERS

15,16 DDR3\_DRAMRST\_N <<-



SAN-1U2NF  
(82.10055.441)



SAN-1U2NF  
(82.10055.441)



## XDP(ITP) for CPU

17,44,58,60 CPU\_CORE\_PWRGD >>>

10 H\_TDO >>>

10 H\_TDS >>>

10 H\_TCK >>>

10 H\_TRST\_N >>>

10 H\_CPUREST\_N >>>

10 H\_PWDY\_N >>>

10,17 H\_PWRGD >>>

10,17,24,51 PLT\_RST\_N >>>

10,17 XDP\_OBRESET\_N >>>

18 CK\_100M\_CPU\_XDP\_DN >>>

18 CK\_100M\_CPU\_XDP\_DP >>>

13 CK\_XDP\_S\_DP >>>

10 CK\_XDP\_S\_DN >>>

18 CK\_PCH\_33M\_P80 >>>

24 LPC\_RST\_N >>>

17,24 LPC\_LAD1 >>>

17,24 LPC\_LAD1 >>>

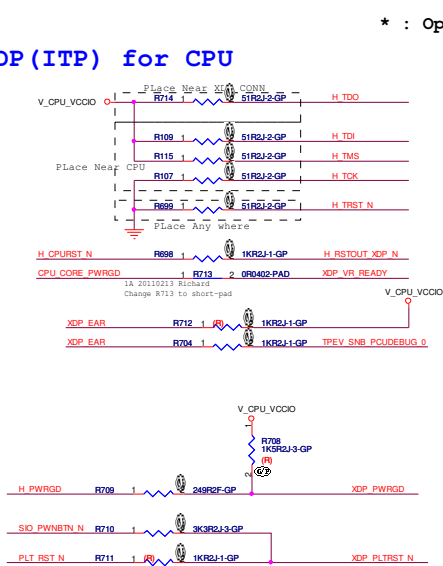
17,24 LPC\_LAD2 >>>

17,24 LPC\_LAD3 >>>

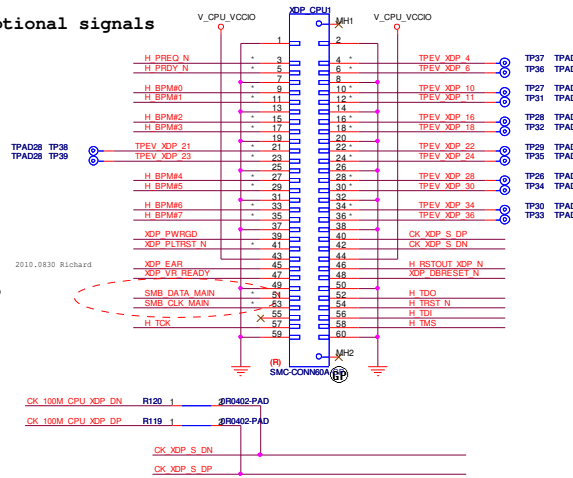
17,24 LPC\_LFRAME\_N >>>

10 TPEV\_SNB\_POUDEBUG\_0 <<<

## XDP(ITP) for CPU



\* : Optional signals



All parts can be placed at back side

## LPC DEBUG PORT

24 SIO\_MCLK >>>

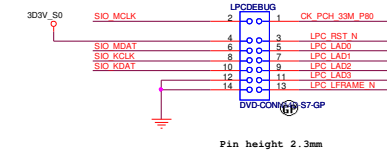
24 SIO\_MDATA >>>

24 SIO\_KCLK >>>

24 SIO\_KDATA >>>

SB 20101222 Richard

Combine SIO F/W PIN



## CRT Header for Debug

SB 20101219 Richard

Remove 0ohm

### From PCH

19 PCH\_HSYNC >>>

19 PCH\_VSYNC >>>

19 PCH\_DDCCLK >>>

19 PCH\_DDCDATA >>>

19 PCH\_RED >>>

19 PCH\_GREEN >>>

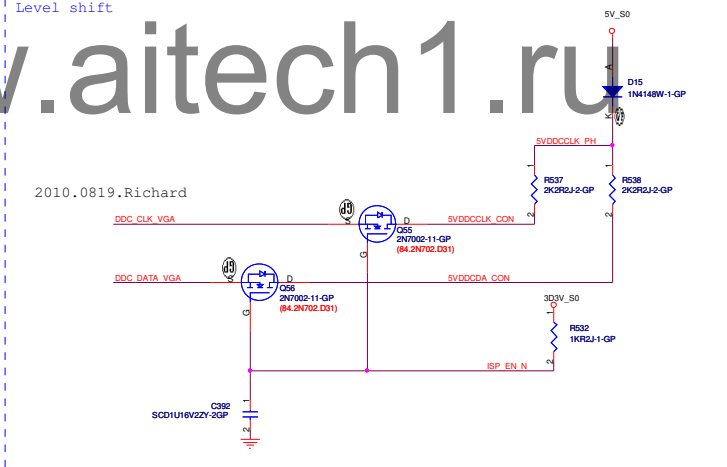
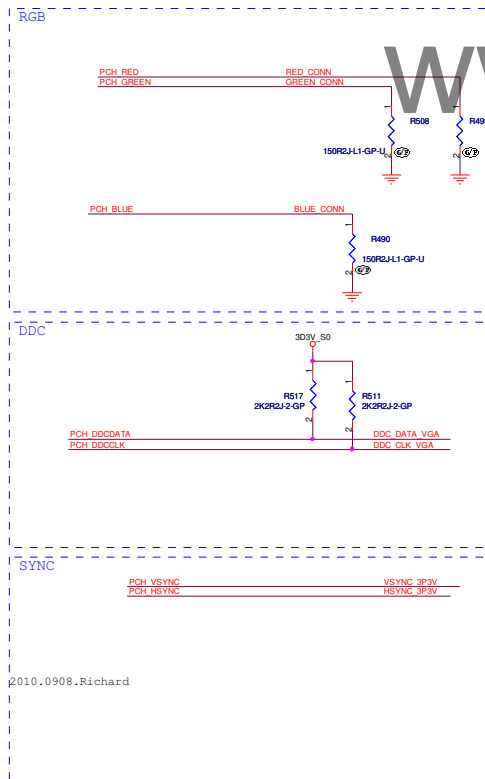
19 PCH\_BLUE >>>

20101102 Richard

Remove R508 R509

20101027 Richard

DEL DEB05 VGA DDC\_CLK DATA



20101011 Richard

CRT Reserve TP

RED CONN TP16 TPA208

GREEN CONN TP19 TPA208

BLUE CONN TP17 TPA208

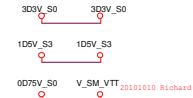
SVDDCLK CONN TP23 TPA208

SVDDCDA CONN TP21 TPA208

VSYSNC 3P3V TP20 TPA208

TSYSNC 3P3V TP18 TPA208

# SSID = MEMORY



## DDR DATA

12 M\_DATA\_A[0:63] <<=

## DDR CMD/ADD

12 M\_MAA\_A[0:15] <<=

## DDR CTRL

12 M\_SBS\_A0 <<=

## DDR CLOCK

12 CK\_M\_DDR0\_A\_DP <<=

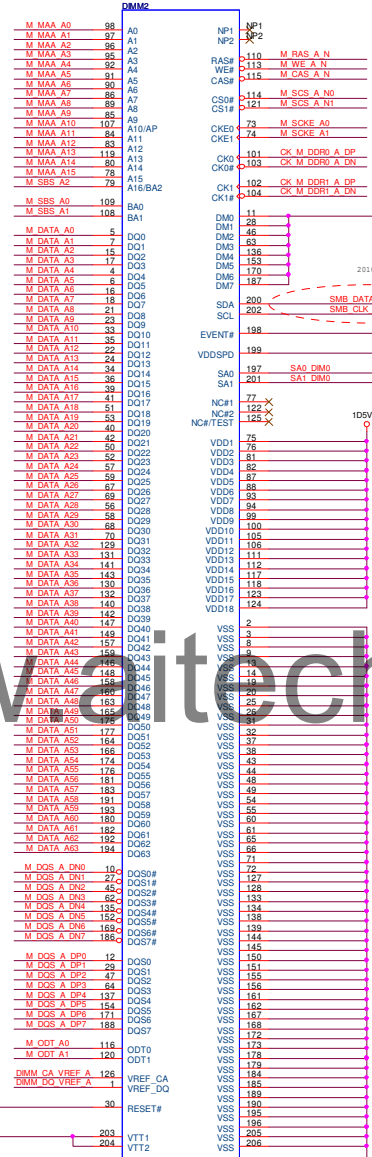
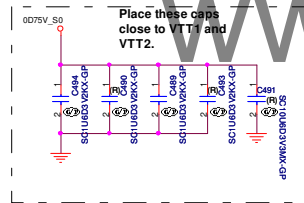
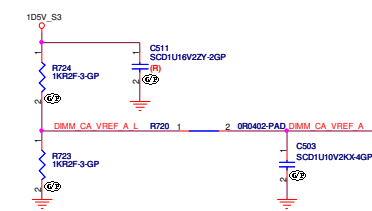
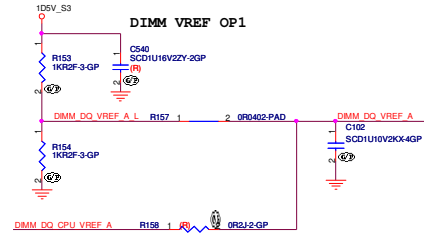
## DDR OTHERS

12,16 DDR3\_DRAMRST\_N <<=

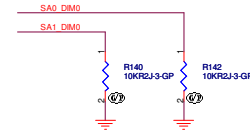
14,16,17,28,58 SMB\_DATA\_MAIN <<=

14,16,17,28,58 SMB\_CLK\_MAIN <<=

13 DIMM\_DQ\_CPU\_VREF\_A <<=



H=9.2mm REV

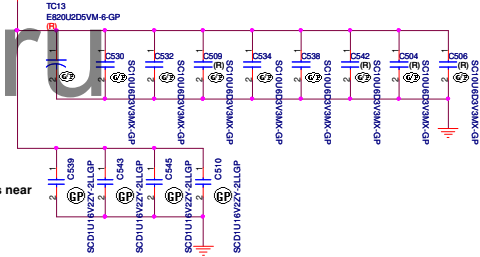


Note:  
If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30  
If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32

## Thermal EVENT



## SODIMM A DECOUPLING



Layout Note:  
Place these Caps near  
SO-DIMMA.

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File	DIMM 1	Rev	SA
Size	Document Number		
C	Tahoe		
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## DDR DATA

12 M\_DATA\_B[0..3]  
12 M\_DQS\_B\_DP[0..7]  
12 M\_DQS\_B\_DN[0..7]

## DDR CMD/ADD

12 M\_MAA\_B[0..15]  
12 M\_WE\_B\_N  
12 M\_CAS\_B\_N  
12 M\_RAS\_B\_N  
12 M\_SBS\_B0  
12 M\_SBS\_B1  
12 M\_SBS\_B2

## DDR CTRL

12 M\_SCS\_B\_N0  
12 M\_SCS\_B\_N1  
12 M\_SCKE\_B0  
12 M\_SCKE\_B1  
12 M\_ODT\_B0  
12 M\_ODT\_B1

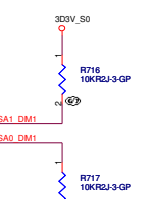
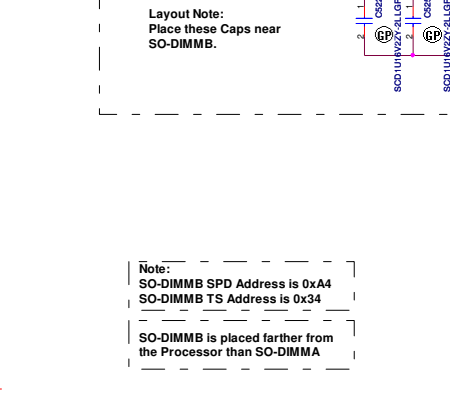
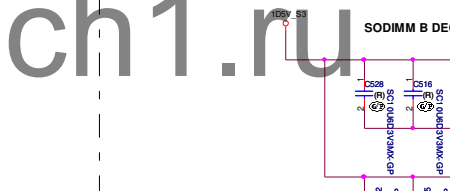
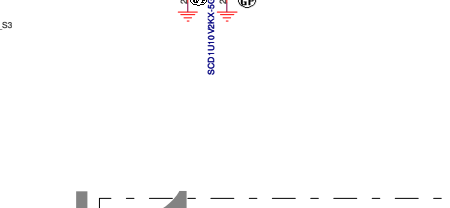
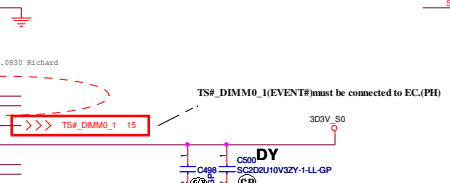
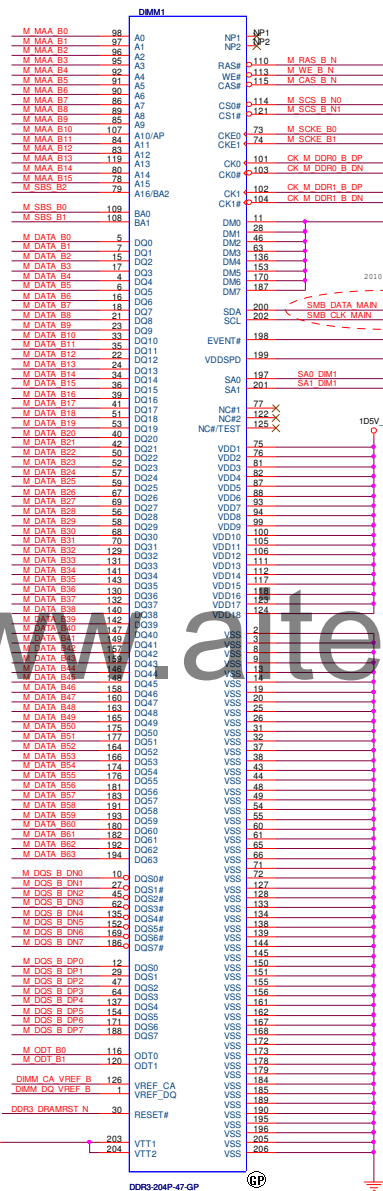
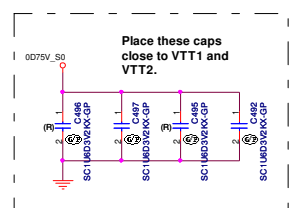
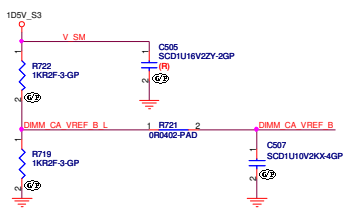
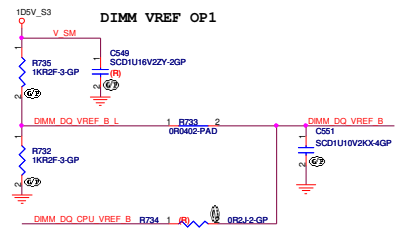
## DDR CLOCK

12 CK\_M\_DDR0\_B\_DP  
12 CK\_M\_DDR0\_B\_DN  
12 CK\_M\_DDR1\_B\_DP  
12 CK\_M\_DDR1\_B\_DN

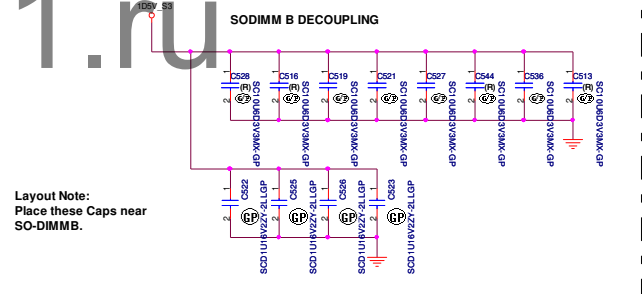
## DDR OTHERS

12,15 DDR3\_DRAMRST\_N

## SSID = MEMORY



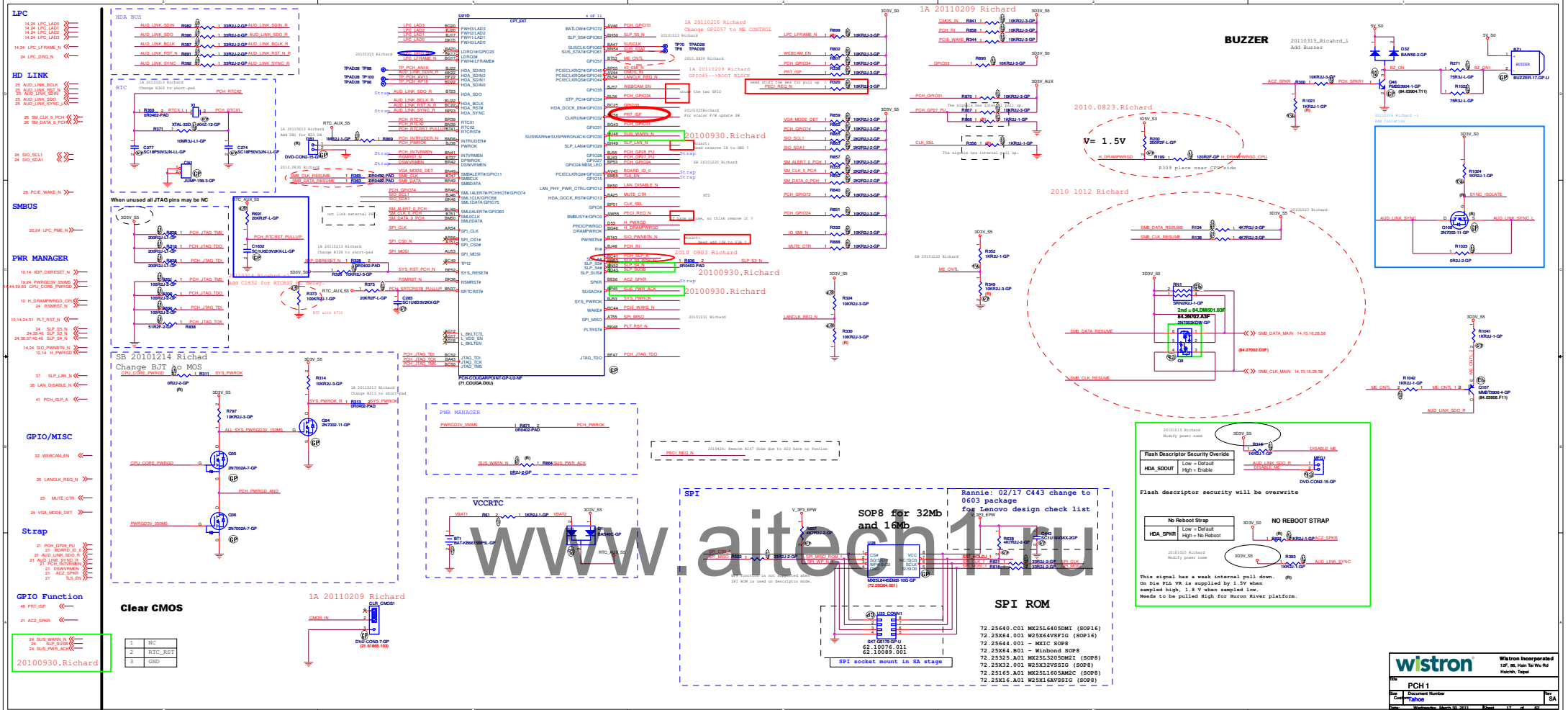
Note:  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34



Layout Note:  
Place these Caps near SO-DIMMB.

Note:  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34  
SO-DIMMB is placed farther from the Processor than SO-DIMMA

H=5.2mm REV





## SATA

29 SATA\_RX0  
29 SATA\_RXP0  
29 SATA\_TX0  
29 SATA\_TXP0  
29 SATA\_RXN1  
29 SATA\_RXP1  
29 SATA\_TXN1  
29 SATA\_TXP1

28 SATA\_RX0  
28 SATA\_RXP0  
28 SATA\_TX0  
28 SATA\_TXP0

PCH\_SATA\_LED\_N

17.24 PWRGD0V\_350MS

41 PCH\_MEWPWOK

## DP PORT B to SCALAR

61 SDVO\_CTRLCLK  
61 SDVO\_CTRLDATA

## VGA

14 PCH\_HSYN  
14 PCH\_VSYN  
14 PCH\_RED  
14 PCH\_GREEN  
14 PCH\_BLUE  
14 PCH\_D0C0DATA  
14 PCH\_D0C0CLK

## OTHERS

24 A20GATE  
21 INT3\_VB  
24 KBRST\_N  
24 INT\_SERRQ  
10 H\_THERMTRIP\_N  
10.24 H\_PECI  
10 H\_PM\_SYNC\_0

## GPIO

32 TP\_DET\_N  
33 CR\_DET  
28 WIFI\_RF\_EN  
32 CAM\_DET\_N

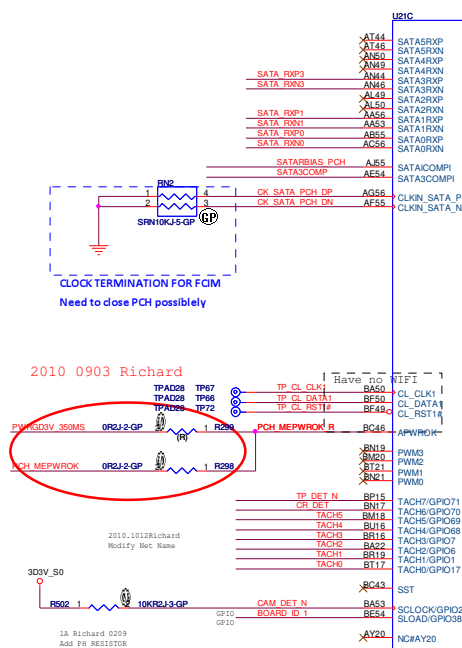
## Strap

21 BOARD\_ID1  
21 SATA3GP  
21 SATA3GP  
21 SATA3GP  
21 NVR\_CLE

## DP PORT D

61 PCH\_CTRL\_CLK  
61 PCH\_CTRL\_DATA

## SST

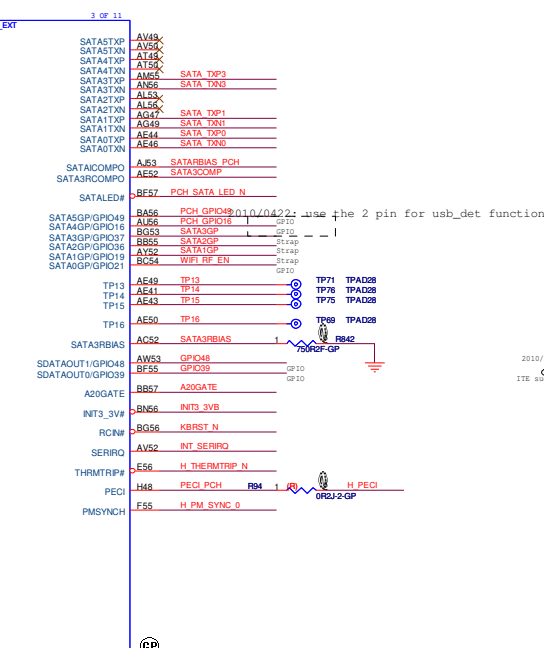


SB 20101201 Richard

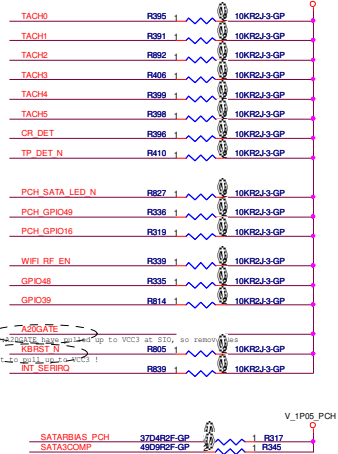
SB 20101201 Richard

Port D: Place near connector

20101028 Richard  
FOR DVI LEVEL SHIFT & AC CAP  
Combine with NVR



## Pull-up on MB



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## PCI CLOCK LOOPBACK

18 CK\_PCH\_33M\_FB

## PWR Manager

## Strap

21 P\_GNT\_N0  
21 P\_GNT\_N1  
21 P\_GNT\_N2  
21 P\_GNT\_N3

24 LPC\_PME\_N

2010.0830 Richard

P\_PORST\_N

## DMI

11 DMI\_CPU\_PCH\_DN0\_3  
11 DMI\_CPU\_PCH\_DP0\_3  
11 DMI\_PCH\_CPU\_DN0\_3  
11 DMI\_PCH\_CPU\_DP0\_3  
10 CK\_DMI\_BUF\_CPU\_DP  
10 CK\_DMI\_BUF\_CPU\_DN

## PCIE

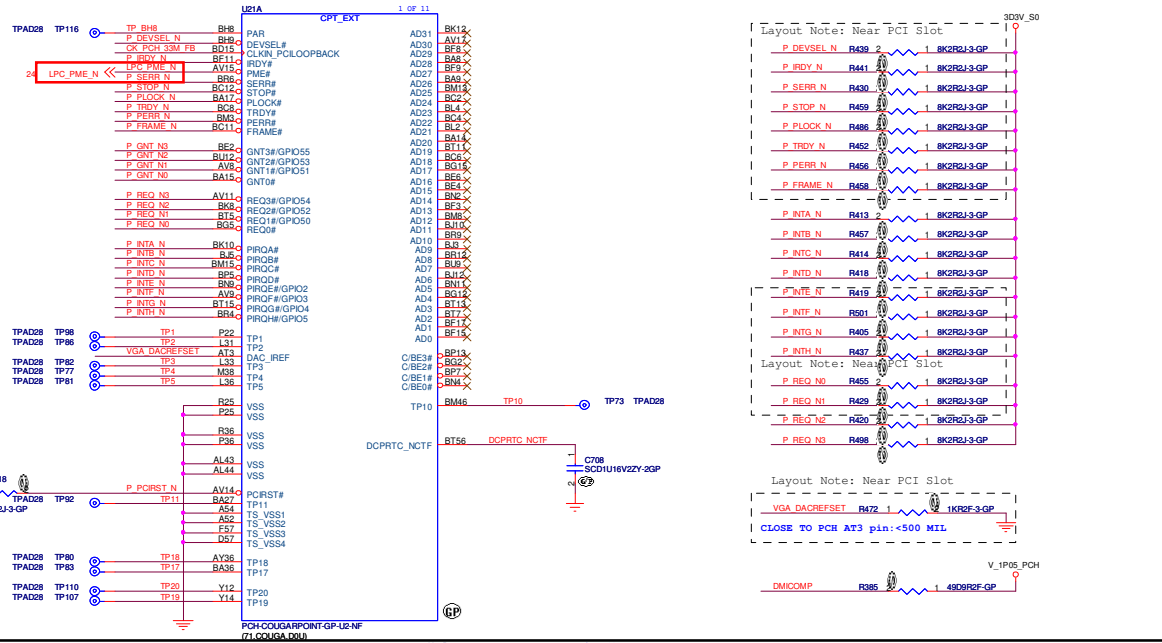
26 PCIE\_RXP1  
26 PCIE\_RXN1  
26 PCIE\_TXP1  
26 PCIE\_TXN1  
26 PCIE\_RXP2  
26 PCIE\_RXN2  
26 PCIE\_TXP2  
26 PCIE\_TXN2

## USB

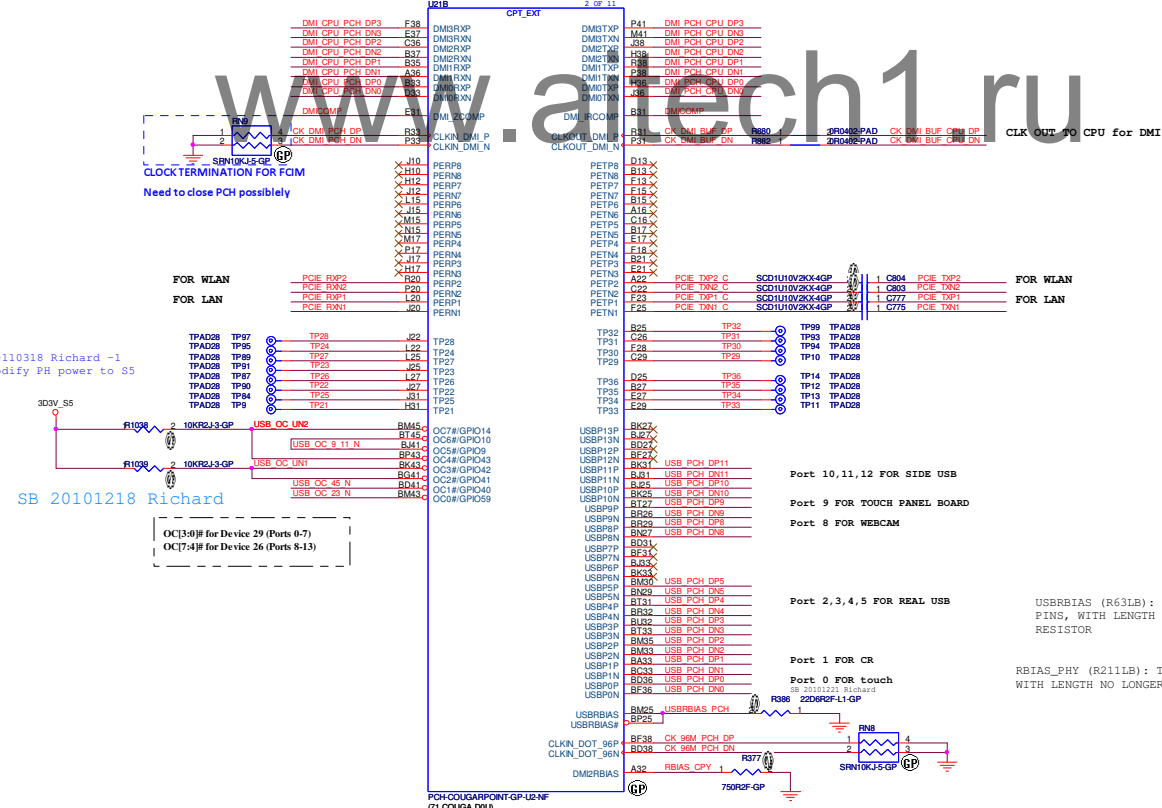
32 USB\_PCH\_DP0  
32 USB\_PCH\_DP1  
32 USB\_PCH\_DP2  
32 USB\_PCH\_DP3  
32 USB\_PCH\_DP4  
32 USB\_PCH\_DP5  
32 USB\_PCH\_DP6  
32 USB\_PCH\_DP7  
32 USB\_PCH\_DP8  
32 USB\_PCH\_DP9  
32 USB\_PCH\_DP10  
32 USB\_PCH\_DP11  
30 USB\_OC\_9\_11\_N  
35 USB\_OC\_45\_N  
35 USB\_OC\_23\_N

## USB OC

30 USB\_OC\_9\_11\_N  
35 USB\_OC\_45\_N  
35 USB\_OC\_23\_N



## DMI/PCIE/USB

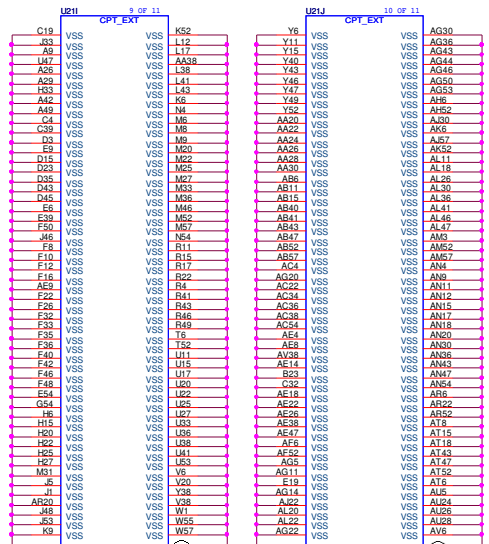


## STRAP

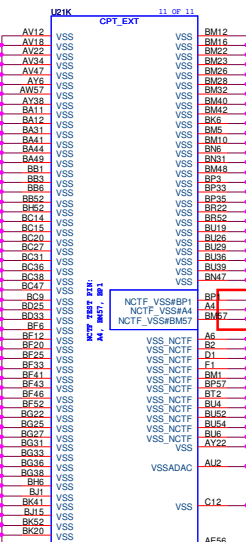
17 ACZ\_SPKR >>  
19 INIT3\_V3B <<  
20 P\_GNT\_N3 <<  
17 PCH\_INTVRMEN <<  
20 P\_GNT\_N2 <<  
20 P\_GNT\_N1 <<  
20 P\_GNT\_N0 <<  
19 NVR\_CLE <<  
17 TLS\_EN >>  
17 AUD\_LINK\_SDO\_R <<  
17 AUD\_LINK\_SYNC\_R <<  
10 H\_SNB\_N >>  
17 PCH\_GP28\_PU >>  
19 SATA1GP <<  
19 SATA2GP <<  
19 SATA3GP <<  
17 DSWVRMEN <<

## BOARD ID

17 BOARD\_ID\_0 <<  
19 BOARD\_ID\_1 <<

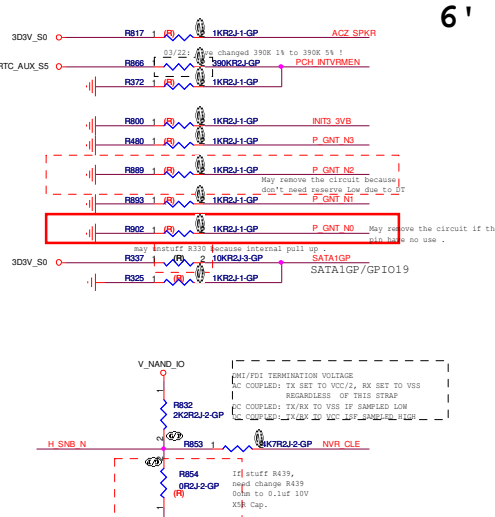


PCH COUGARPOINT-GP-L2-NF (71.COUGA.D0U)  
PCH COUGARPOINT-GP-L2-NF (71.COUGA.D0U)



PCH COUGARPOINT-GP-L2-NF (71.COUGA.D0U)

BOOT DEVICE	GNT1	SATA1GP / GPIO19
SPI	1	1
PCI	1	0
FWH	0	0



## 6' serial strapping define

## PCH Functional Straps

PCH EDS, Page89, Table 89-93

SPKR	The signal has a weak internal pull-down. Note: The internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:Bit 5).
PCH_INTVRMEN	Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high
INIT3_V3B	This signal has a weak internal Res=20K pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low
P_GNT_N3	Top-Block Swap Override The signal has a weak internal Res=20K pull-up. If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode
P_GNT_N2	This Signal has a weak internal Res=20K pull-up. NOTE: The internal pull-up is disabled after PLTRST# deasserts. Tying this strap low configures DMI for ESI compatible operation. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
P_GNT_N1	Boot BIOS Destination Selection Signal has weak internal Res=20K pull-ups.
SATA1GP/GPIO19	Boot BIOS Destination Selection Signal has weak internal Res=20K pull-ups.
NVR_CLE	DMI and FDI Tx/Rx Termination Voltage The signal has a weak internal Res=20K pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
AUD_LINK_SDO_R	The signal has a weak internal Res=20K pull-down. Flash Descriptor Security Override Strap. In Page92 ESD.
AUD_LINK_SYNC_R	The signal has a weak internal Res=20K pull-down. On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low. In Page92 ESD.
PCH_GP28_PU	This signal has a weak internal Res=20K pull-up. NOTE: The internal pull-up is disabled after RSMRST# deasserts. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.
TLS_EN (GPIO15)	The signal has a weak internal Res=20K pull-down. NOTE: The weak internal pull-down is disabled after RSMRST# deasserts. Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality NOTE: A strong pull-up may be needed for GPIO functionality
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
FB_USB2_DET	DMI RX TERMINATION VOLTAGE OVERRIDE This signal has a weak internal Res=20K pull-down
SATA3GP	FDI RX TERMINATION VOLTAGE OVERRIDE This signal has a weak internal Res=20K pull-down

## Board ID (Page17,19)

[4..1]	
1101	
1001	
1000	
0001	
0011	

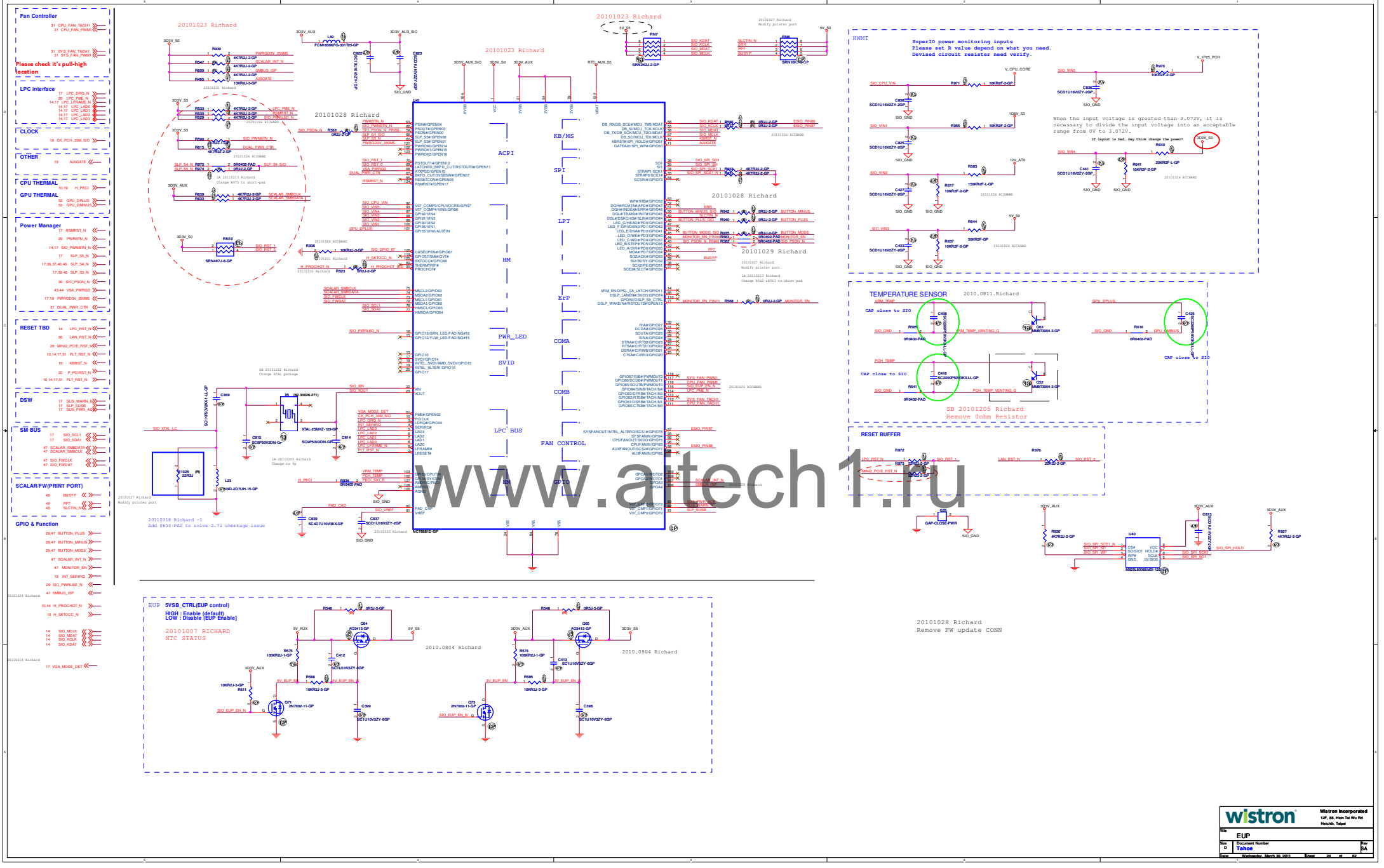
wistron

Wistron Incorporated  
12F, 88, Hsin Tai Wu Rd  
Hsinchu, Taipei

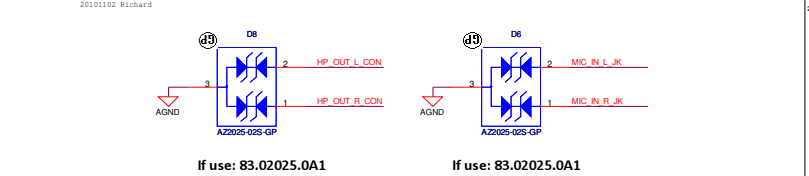
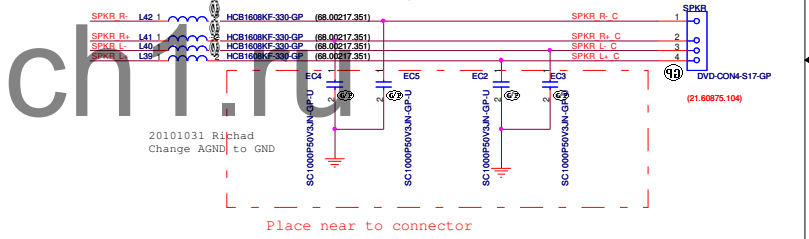
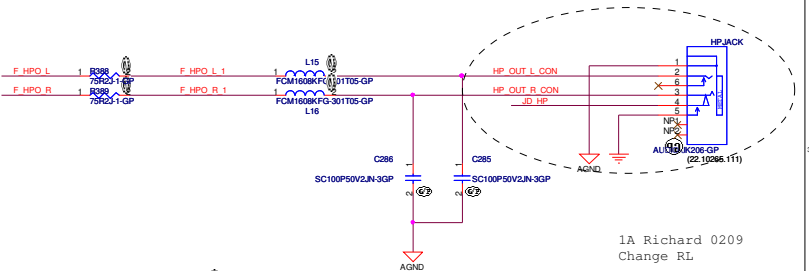
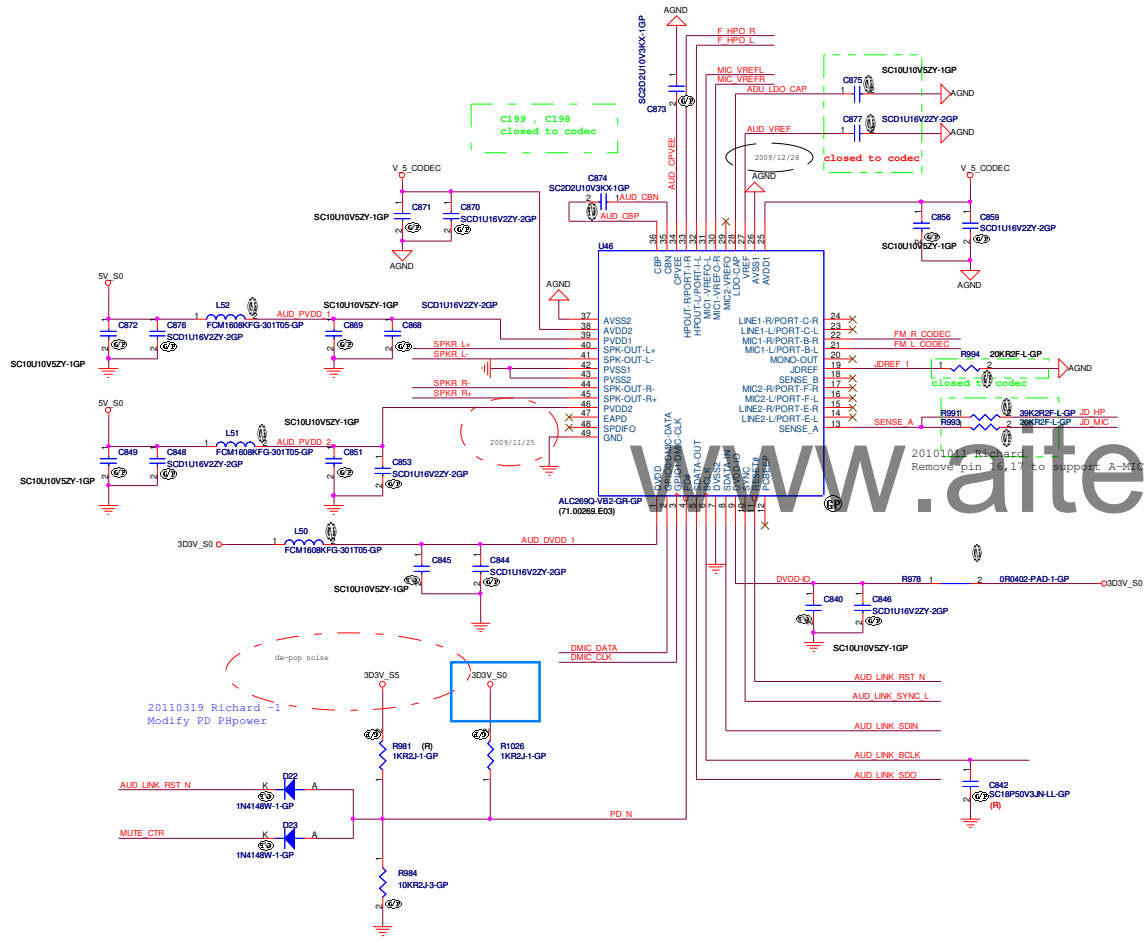
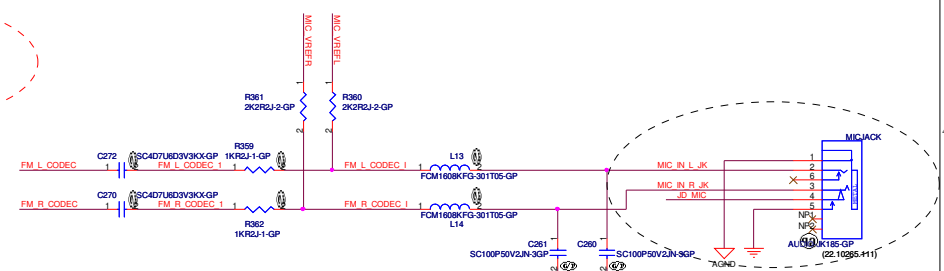
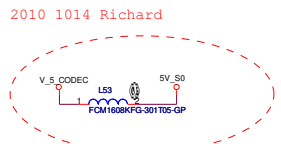
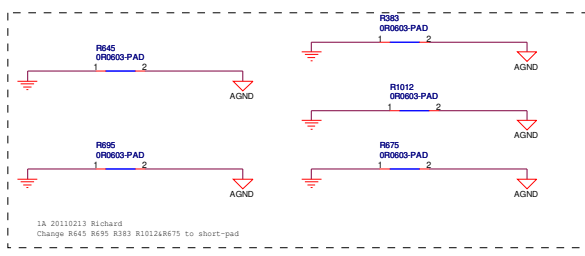
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Size: C  
Document Number: Tahoe  
Date: Wednesday, March 30, 2011  
Sheet: 21 of 62  
New SA



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17 AUD\_LINK\_BCLK  
17 AUD\_LINK\_SDM  
17 AUD\_LINK\_SYNC\_L  
17 AUD\_LINK\_RST\_N  
17 AUD\_LINK\_SDO  
32 DMIC\_DATA  
32 DMIC\_CLK  
17 MUTE\_CTR

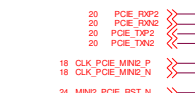




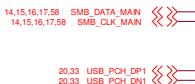
www.aitech1.ru

		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsinchu, Taipei	
Title RESERVE			
Size C	Document Number Tahoe		Rev SA
Date: Wednesday, March 30, 2011		Sheet	27 of 62

# WLAN

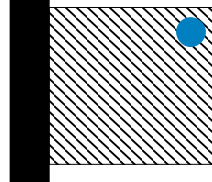


# SMBUS

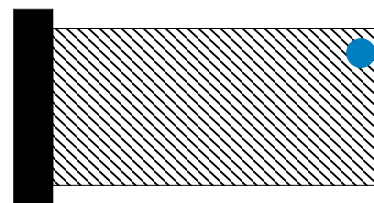


## Mini PCI-E Connector

### Half Mini PCI-E CARD

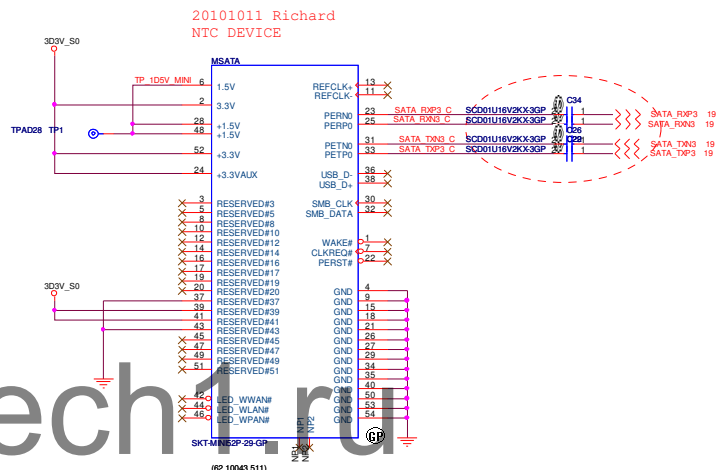
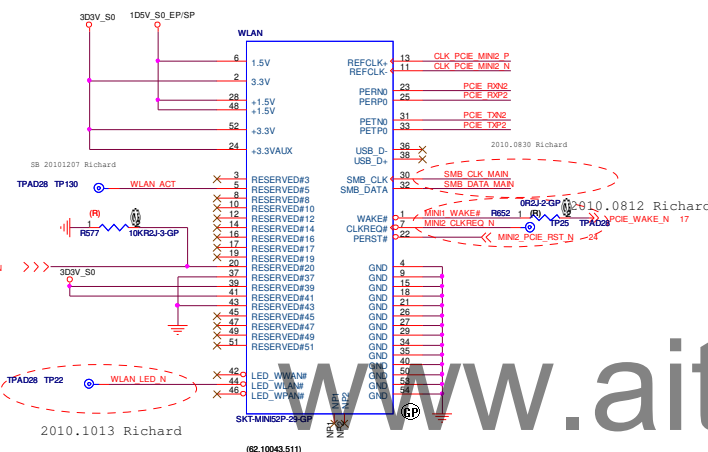
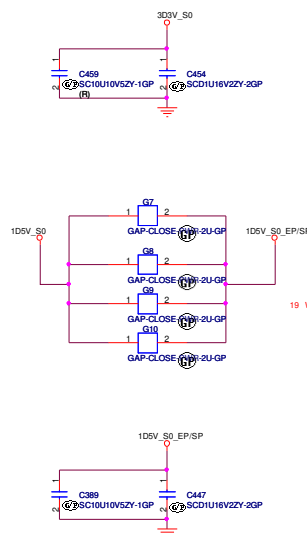


### Full Mini PCI-E CARD

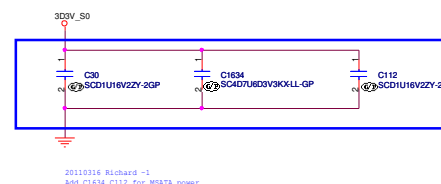
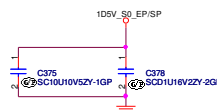
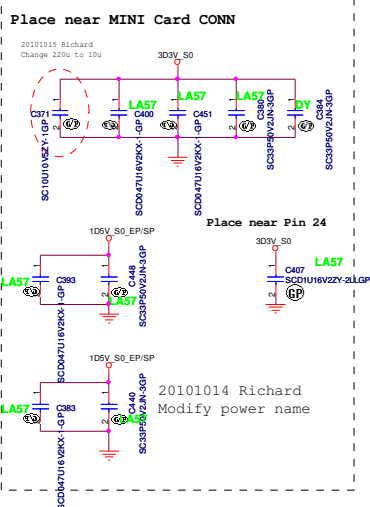


## Mini Card Connector(Wireless LAN)

## Mini Card Connector(mSATA SSD)



## SSID = Wireless



<Variant Name>

**wlstron**

Wistron Incorporated  
21F, 88, Hei Tai Wu Rd  
Heichih, Taipei

Title: MINI PCIE  
Size: C Document Number: New  
Date: Wednesday, March 30, 2011 Sheet: 28 of 62

## POWER\_BTN to SIO

24 PWRBTN\_N  
24 SIO\_PWLED\_N

## BUTTON key to SCALAR

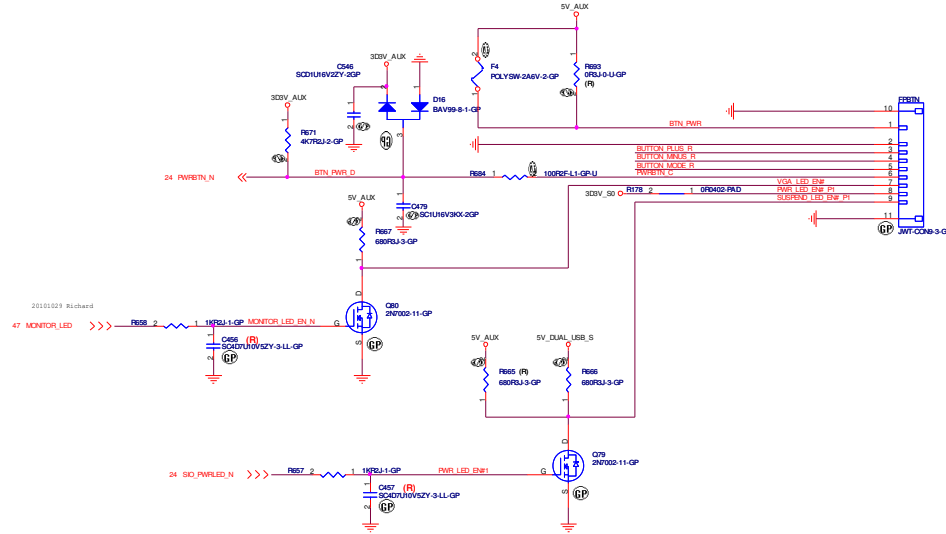
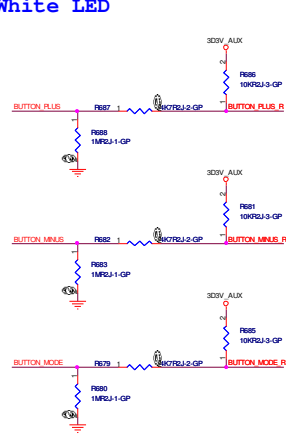
24:47 BUTTON\_PLUS  
24:47 BUTTON\_MINUS  
24:47 BUTTON\_MODE

## PCH SATA

19 SATA\_P0N0  
19 SATA\_P0P0  
19 SATA\_T0N0  
19 SATA\_T0P0

19 SATA\_P0N1  
19 SATA\_P0P1  
19 SATA\_T0N1  
19 SATA\_T0P1

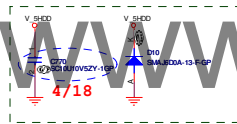
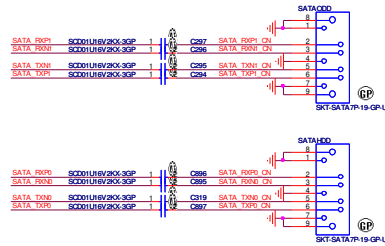
47 MONITOR\_LED  
20101029 Richard

PWRBTN BUTTON with  
White LED

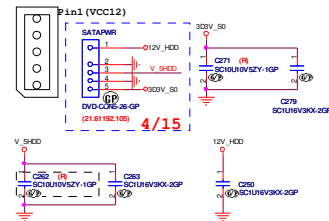
## SATA CONNECTORS

SB 120808 Richard  
SWAP SATA PORT

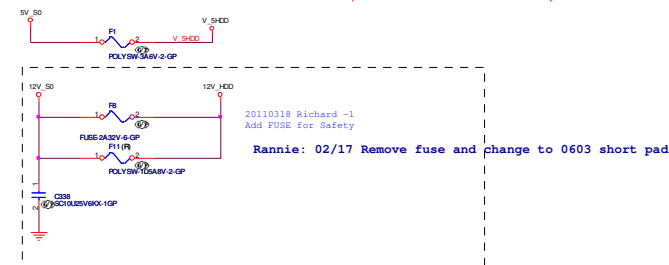
1A 20110216 Richard  
Remove SATA Driver IC



Layout: Please put them together



20101013 Richard



<Variant Name>

**wistron**

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Heilshih, Taipei

File	BTN SATA	Rev	SA
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Custom	Tahoe		
Date	Wednesday, March 30, 2011	Sheet	29 of 62

USB Power Enable

24,36,37,40,46 SLP\_S4\_N >>>

USB signal

20 USB\_PCH\_DP11

20 USB\_PCH\_DN11

20 USB\_PCH\_DP9

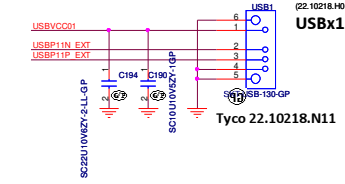
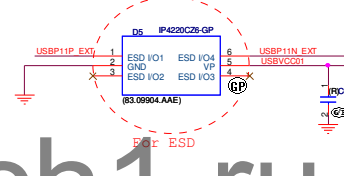
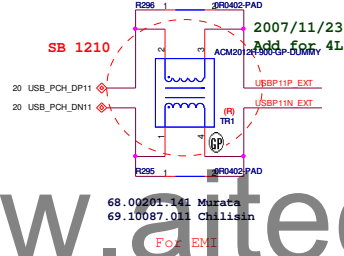
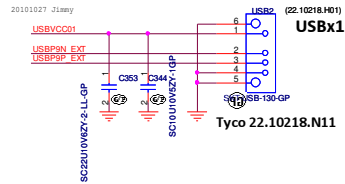
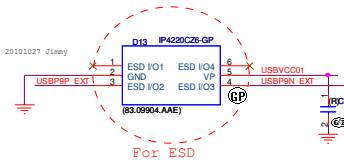
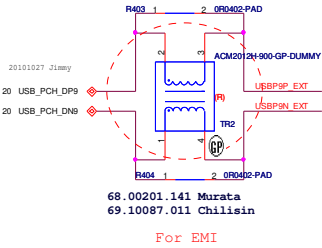
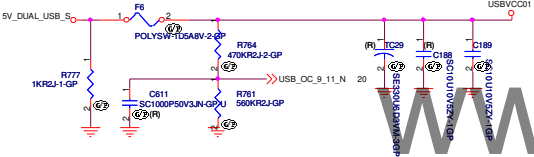
20 USB\_PCH\_DN9

20 USB\_OC\_9\_11\_N <<<

USB Power (S0,S3)

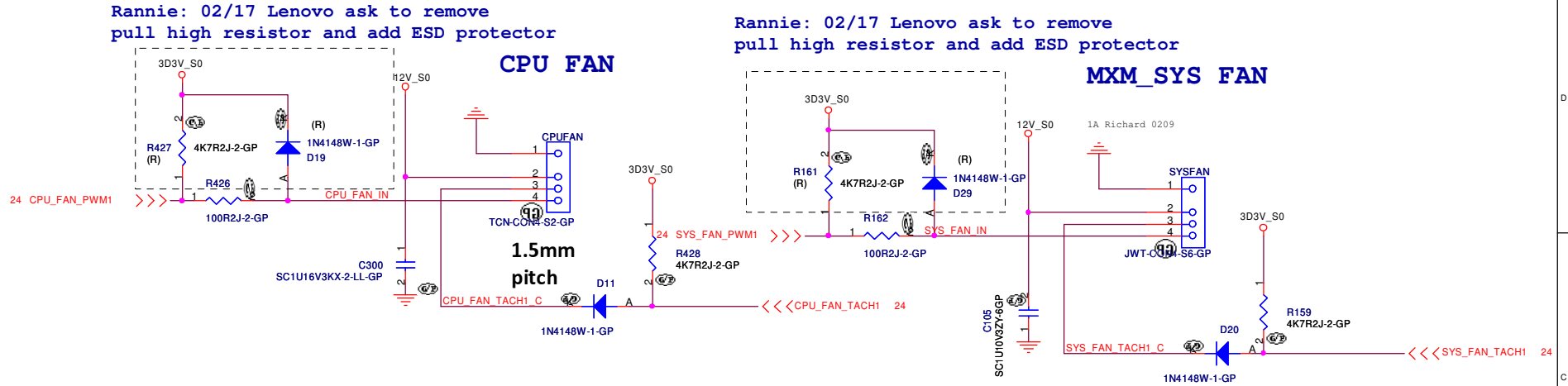
2010.0811 Richard

Use 69.50007.801 (Littelfuse)



# SIO FAN CONTROL

24 CPU\_FAN\_TACH1  
24 CPU\_FAN\_PWM1  
24 SYS\_FAN\_TACH1  
24 SYS\_FAN\_PWM1



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SB 20101207 Richard  
Remove PSU FAN

<Variant Name>

<b>wistron</b>			<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
<b>FAN</b>			
Title	Document Number <b>Tahoe</b>	Rev SA	
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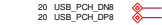
WEBCAM



Touch Panel



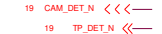
BlueTooth



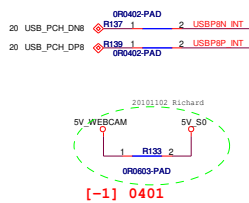
LED



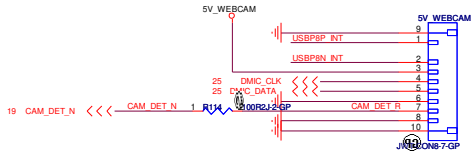
NTD



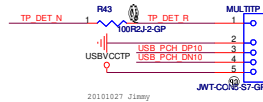
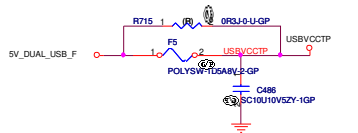
WEBCAM



[-1] 0401



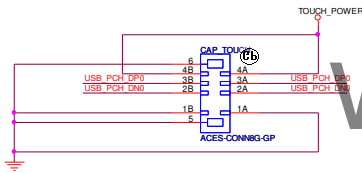
Touch Panel



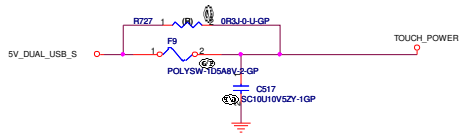
BTRF

RF->Wireless  
KB/MS  
REMOVE!!

20110322 Richard -1  
SWAP pin define



Blue Tooth  
Power



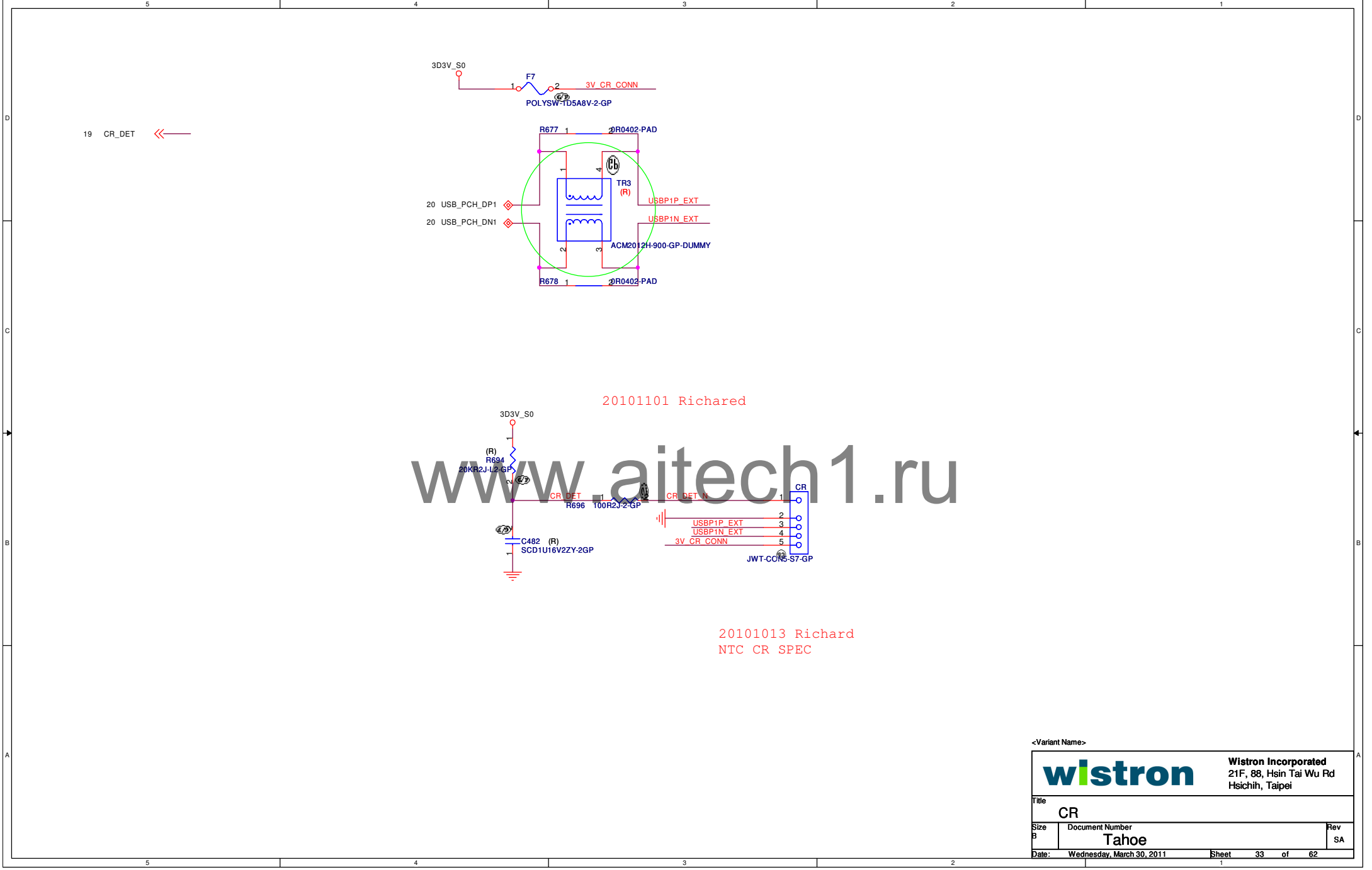
LED

20101007 Richard  
DEL BT,WLAN,HDD LED

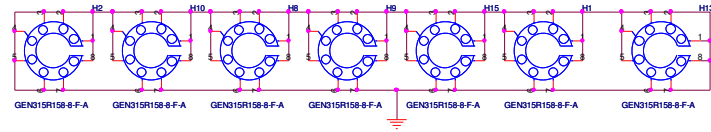
www.aitech1.ru

<Core Design>

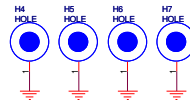
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
File		CAMER BT TOUCH	
Size	Document Number		Rev
C		Tahoe	SA
Date: Wednesday, March 30, 2011		Sheet 32	of 62



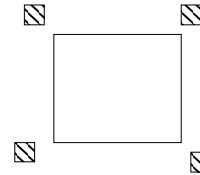
### PCB MOUNTING HOLES-PTH



### HOLE205R158



### CPU MOUNTING HOLE-PTH



### MINI PCIE 1 MOUNTING HOLE-PTH

### MINI PCIE 1 MOUNTING HOLE-PTH

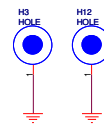
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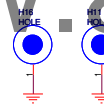
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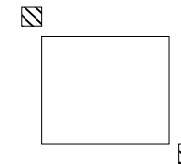
### HOLE197R102



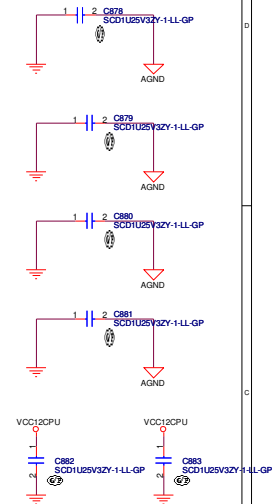
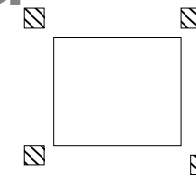
### HOLE197R122



### PCH MOUNTING HOLE-PTH



### GPU MOUNTING HOLE-PTH



### PCH MOUNTING HOLE-PTH

### SYS FAN HOLE-PTH

<Variant Name>

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21F, 88, Hei Tai Wu Rd  
Hsichih, Taipei

Title

SCALAR FW

Size

Document Number

Tahoe

Rev

SA

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## Display Port

61 DDSP\_D\_TX\_DP\_0 <<<  
61 DDSP\_D\_TX\_DP\_1 <<<  
61 DDSP\_D\_TX\_DP\_2 <<<  
61 DDSP\_D\_TX\_DP\_3 <<<  
61 DDSP\_D\_TX\_DP\_4 <<<  
61 DDSP\_D\_TX\_DP\_5 <<<  
61 DDSP\_CTRL\_CLK <<<  
61 DDSP\_CTRL\_DATA <<<  
61 DDSP\_D\_HPD <<<

## VGA Port

62 RED\_IN\_CONN <<<  
62 GREEN\_IN\_CONN <<<  
62 BLUE\_IN\_CONN <<<  
62 HSYNC\_IN\_CONN <<<  
62 VSYNC\_IN\_CONN <<<  
47.62 CRT\_DDC\_IN\_CLK <<<  
47.62 CRT\_DDC\_IN\_DATA <<<

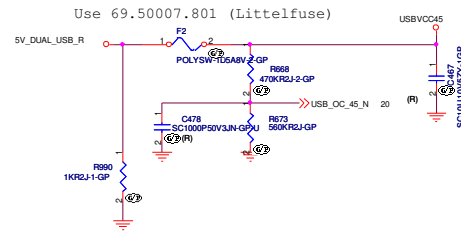
## USB Port

20 USB\_PCH\_DP2 <<<  
20 USB\_PCH\_DP3 <<<  
20 USB\_PCH\_DP4 <<<  
20 USB\_PCH\_DP5 <<<  
20 USB\_PCH\_DP6 <<<  
20 USB\_PCH\_DP7 <<<

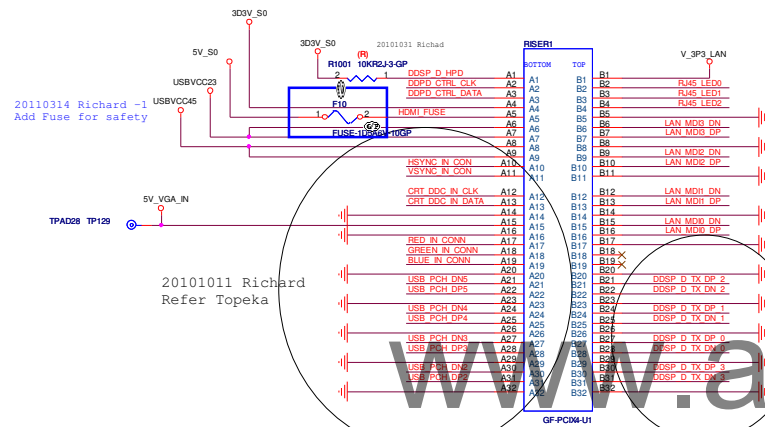
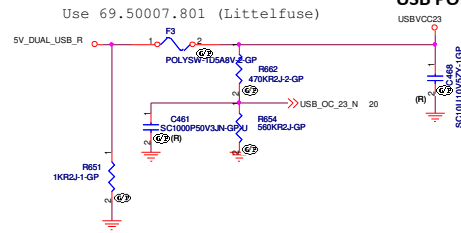
## LAN Port

26 RU45\_LED0 <<<  
26 RU45\_LED1 <<<  
26 RU45\_LED2 <<<  
26 LAN\_MDIO\_DN <<<  
26 LAN\_MDIO\_DP <<<  
26 LAN\_MDIO\_DN <<<  
26 LAN\_MDIO\_DP <<<  
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26 LAN\_MDIO\_DP <<<

## USB PORT4/5 Power



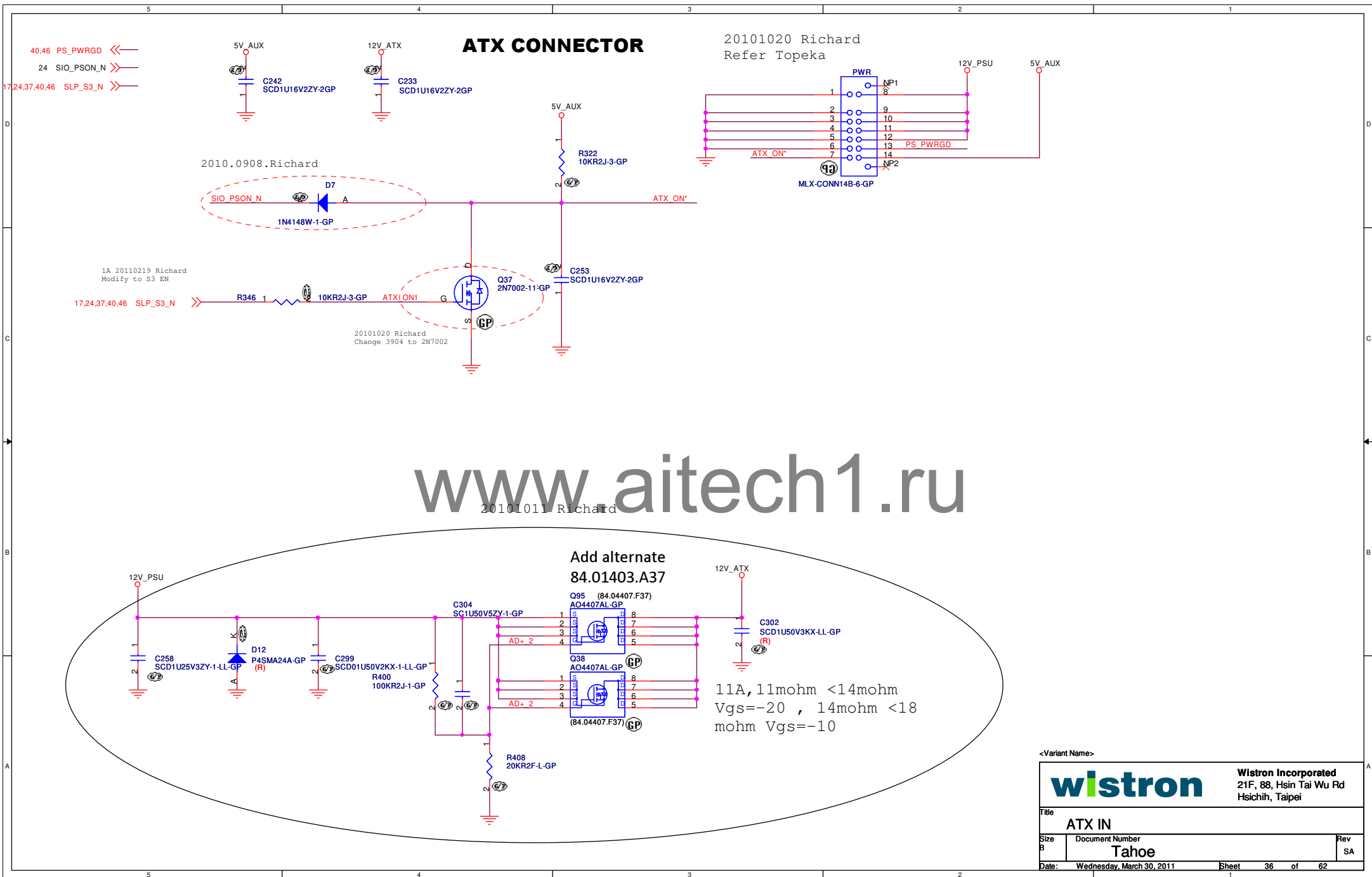
## USB PORT2/3 Power



20101011 Richard  
Don't support Display port

20101027 Richard  
Refer RISER

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<Variant Name>

**wistron**

**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title

**ATX IN**

Size

Document Number

**Tahoe**

Rev

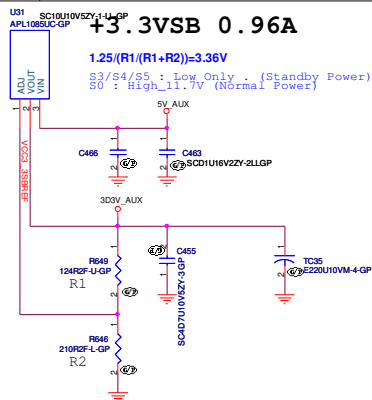
SA

Date: Wednesday, March 30, 2011

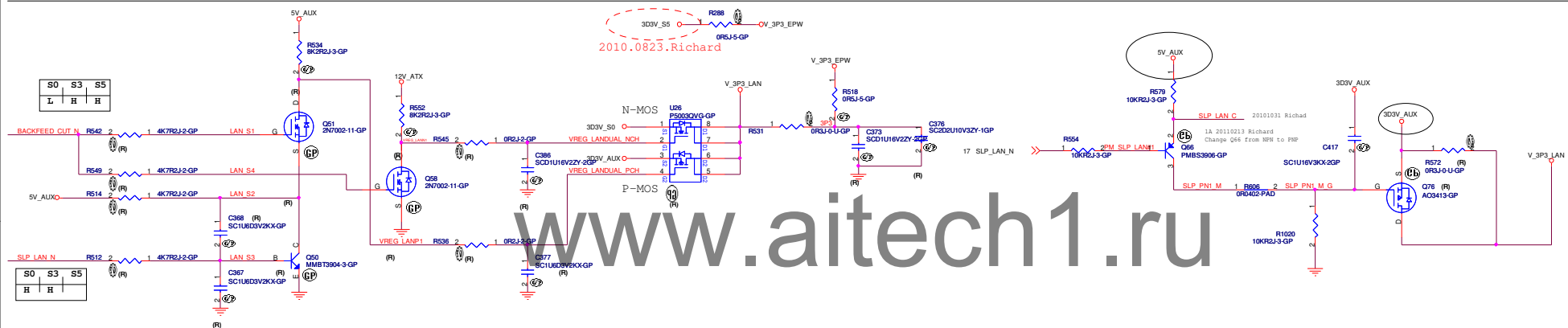
Sheet 36 of 62

SB 20101203 Richard

38,41,46,60 PC\_PWRGD >>  
46 LATCHED\_BACKFEED\_CUT >>  
17 SLP\_LAN\_N >>  
46 BACKFEED\_CUT\_N >>  
24 DUAL\_PWR\_CTR >>  
17,24,36,40,46 SLP\_S4\_N >>



## V\_3P3\_LAN/EPW DUAL

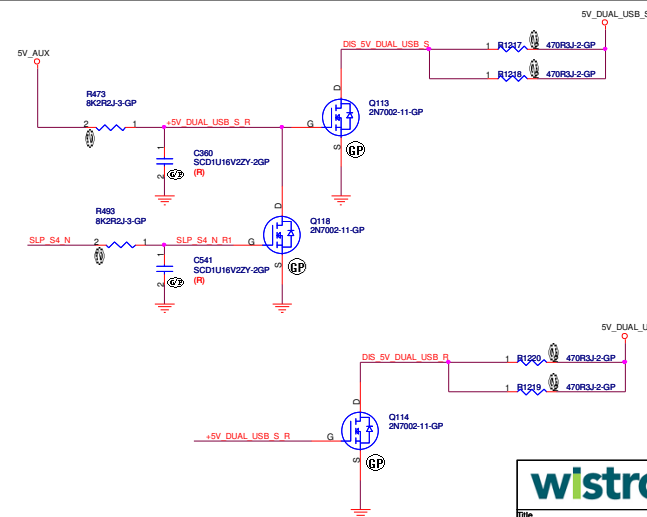
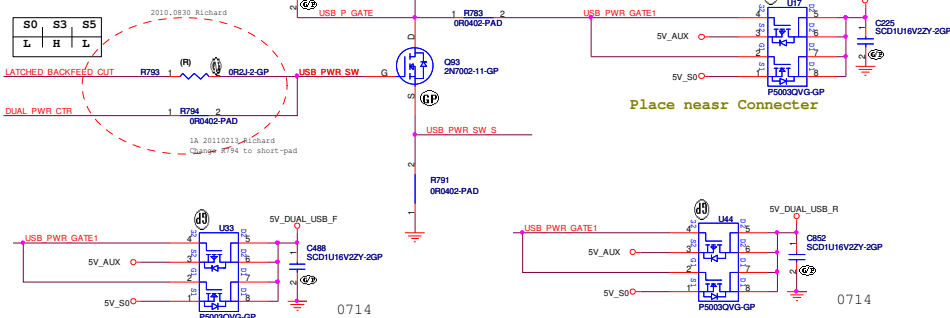


## 5V\_DUAL USB CONTROL

20101028 Richard  
Remove USB charger power

## SIDE USB PWR

Place nears Connector



## FRONT USB PWR

## REAR USB PWR

# +3VSB/+5VSB

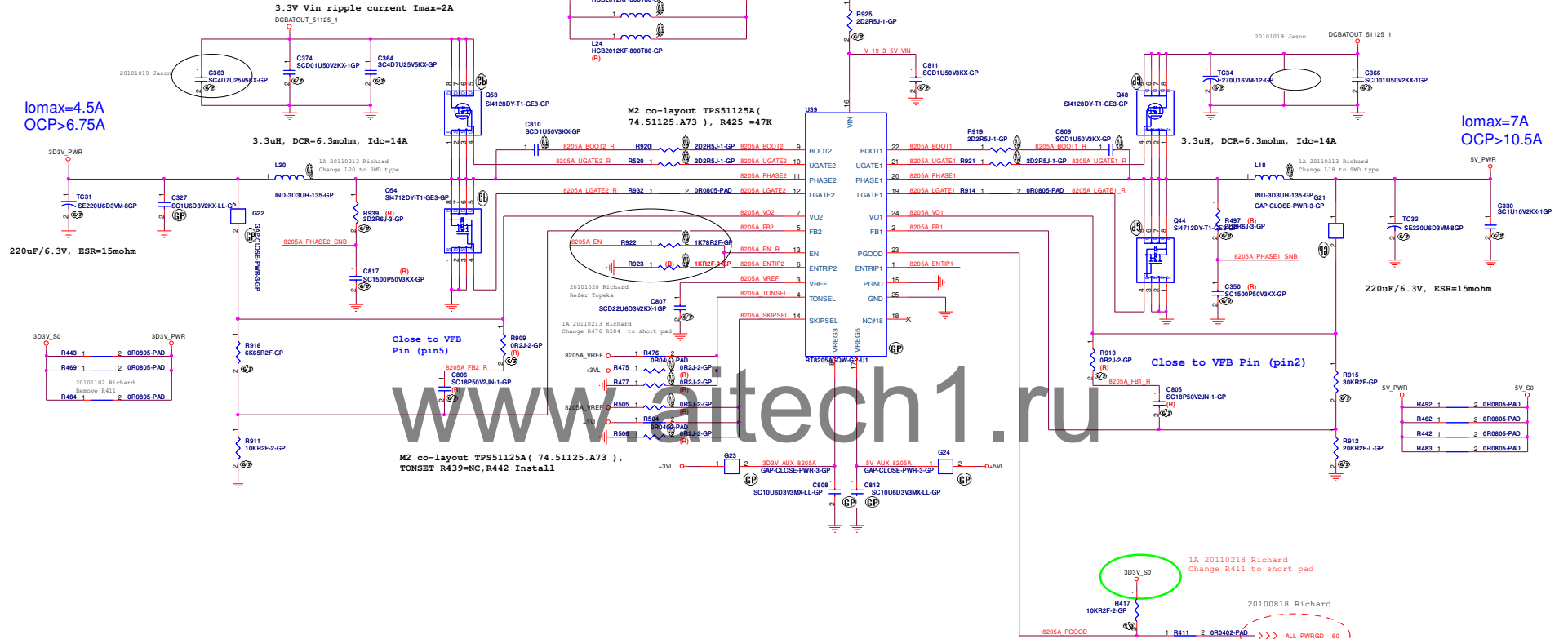
84.04128.037 SI4128DYP  
Vgs @ 4.5V,  
Id = 6.0A,  
Rds(on) = 24.0~30.0mohm,  
Qg = 3.8~6.0nC

84.04712.A37 SI4712DY  
Vgs @ 4.5V,  
Id = 8.2A,  
Rds(on) = 13.0~16.5mohm,  
Qg = 8.3~12.5nC

5V Vin ripple current Imax=3.45A

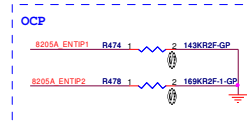
84.04128.037 SI4128DYP  
Vgs @ 4.5V,  
Id = 6.0A,  
Rds(on) = 24.0~30.0mohm,  
Qg = 3.8~6.0nC

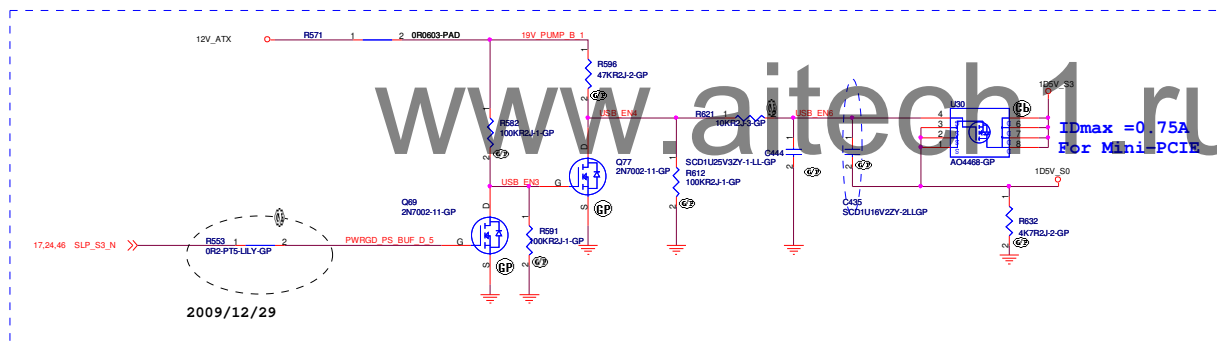
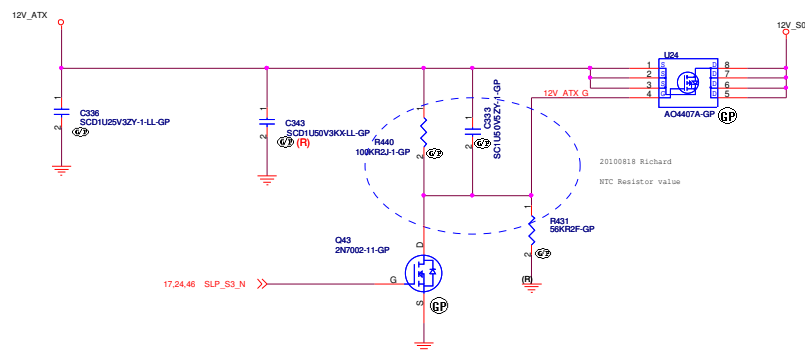
84.04712.A37 SI4712DY  
Vgs @ 4.5V,  
Id = 8.2A,  
Rds(on) = 13.0~16.5mohm,  
Qg = 8.3~12.5nC



RT8205A	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	SKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	330k/CH1 375k/CH2	400k/CH1 500k/CH2	400k/CH1 500k/CH2

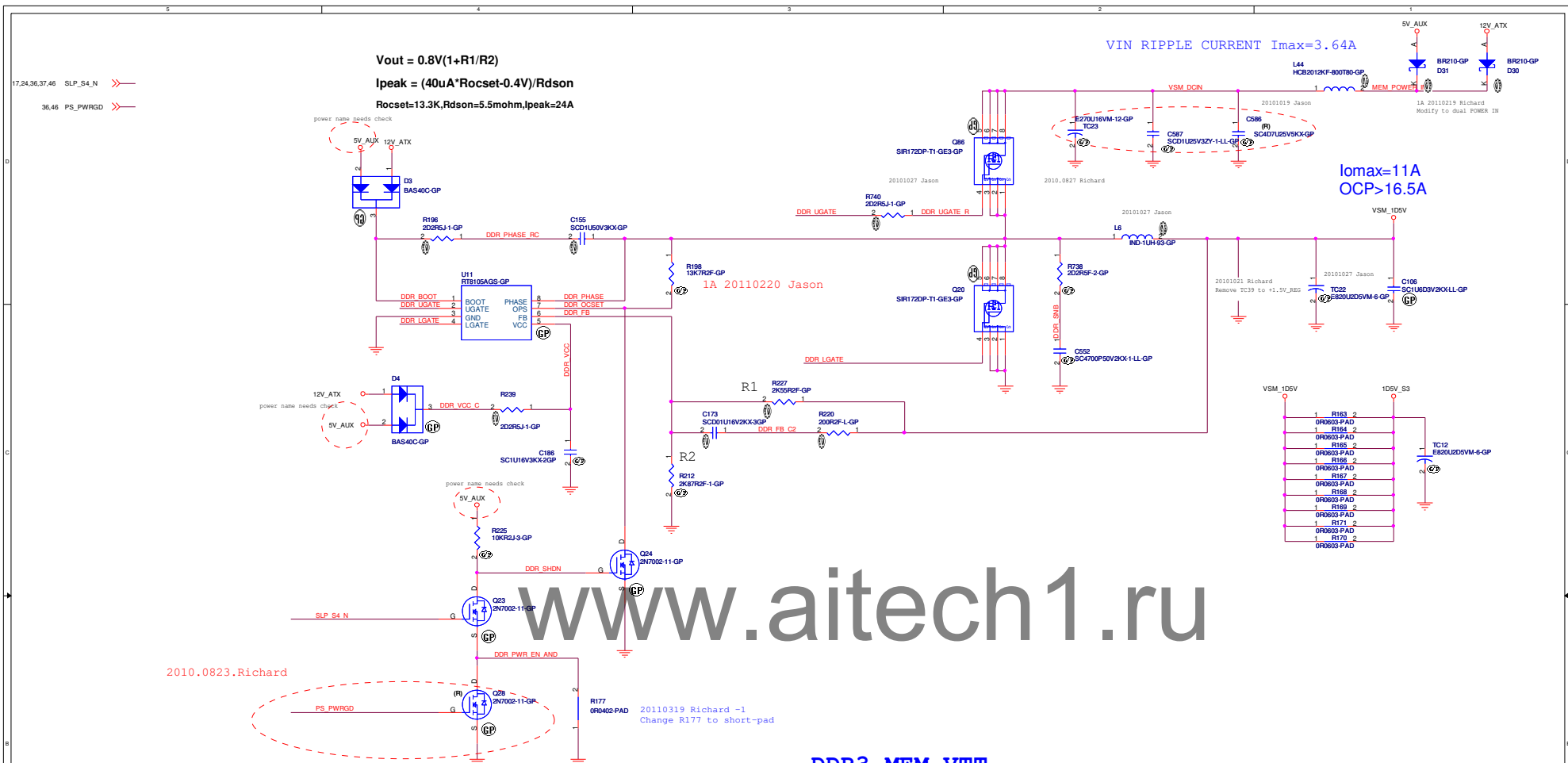
TPS51125A	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	SKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2



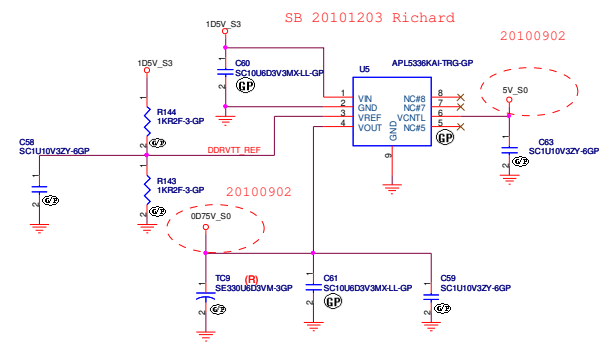


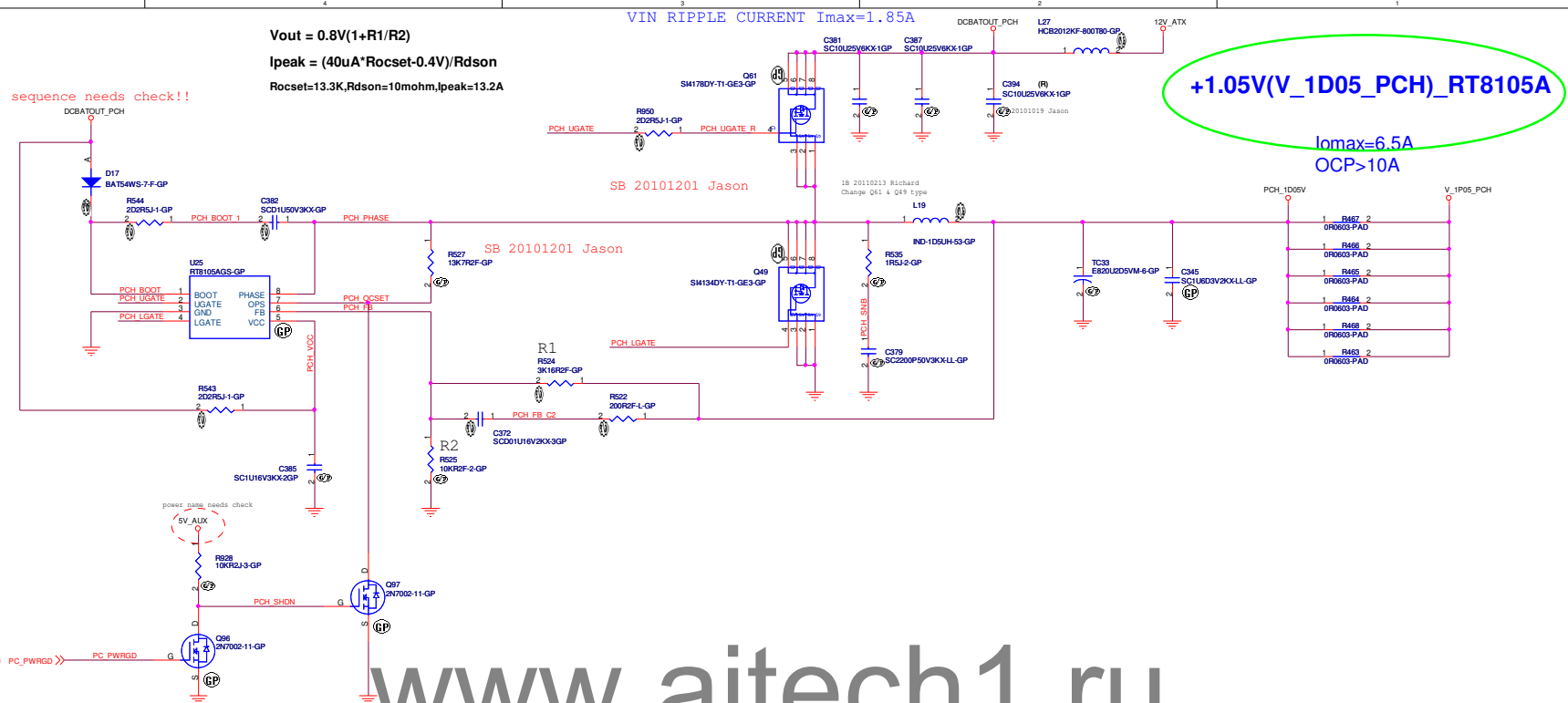
<Variant Name>

<b>wistron</b>		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title <b>RUN POWER</b>			
Size C	Document Number <b>Tahoe</b>		Rev SA
Date:	Wednesday, March 30, 2011	Sheet	39 of 62

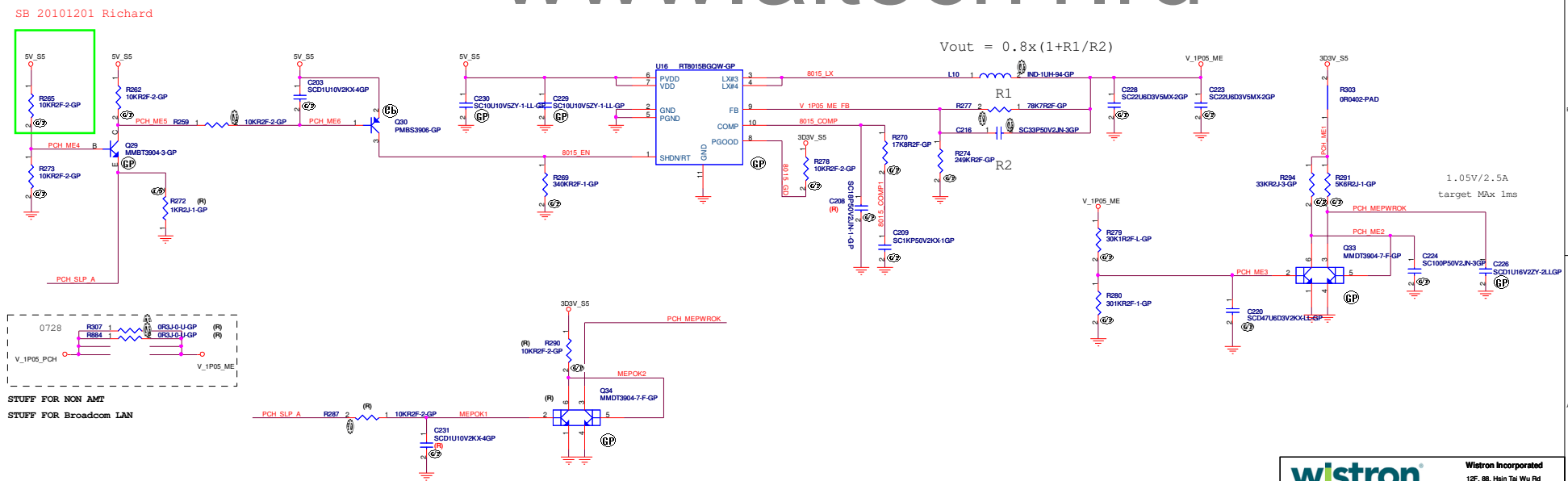


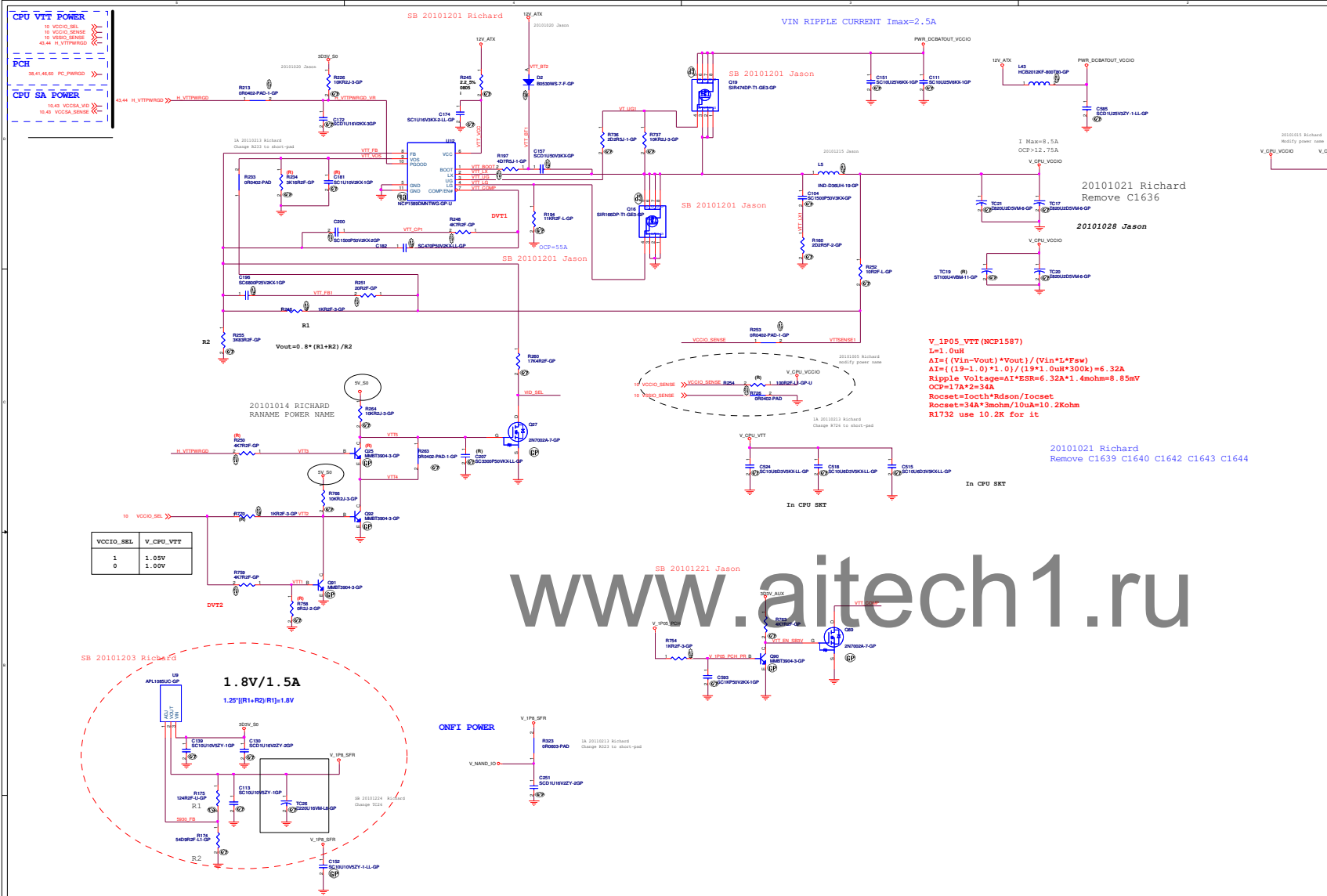
**DDR3\_MEM\_VTT**  
**0D75V\_Iomax=1.5A**





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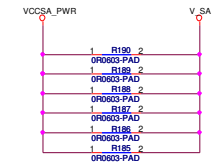




**+0.85V(0D85V\_S0)\_APL5611 for VCCSA**

SB 20101208  
Change Power Solution

10 VOCSA\_VID >>—



VID	V_SA
0	0.925V(Default)
1	0.85V

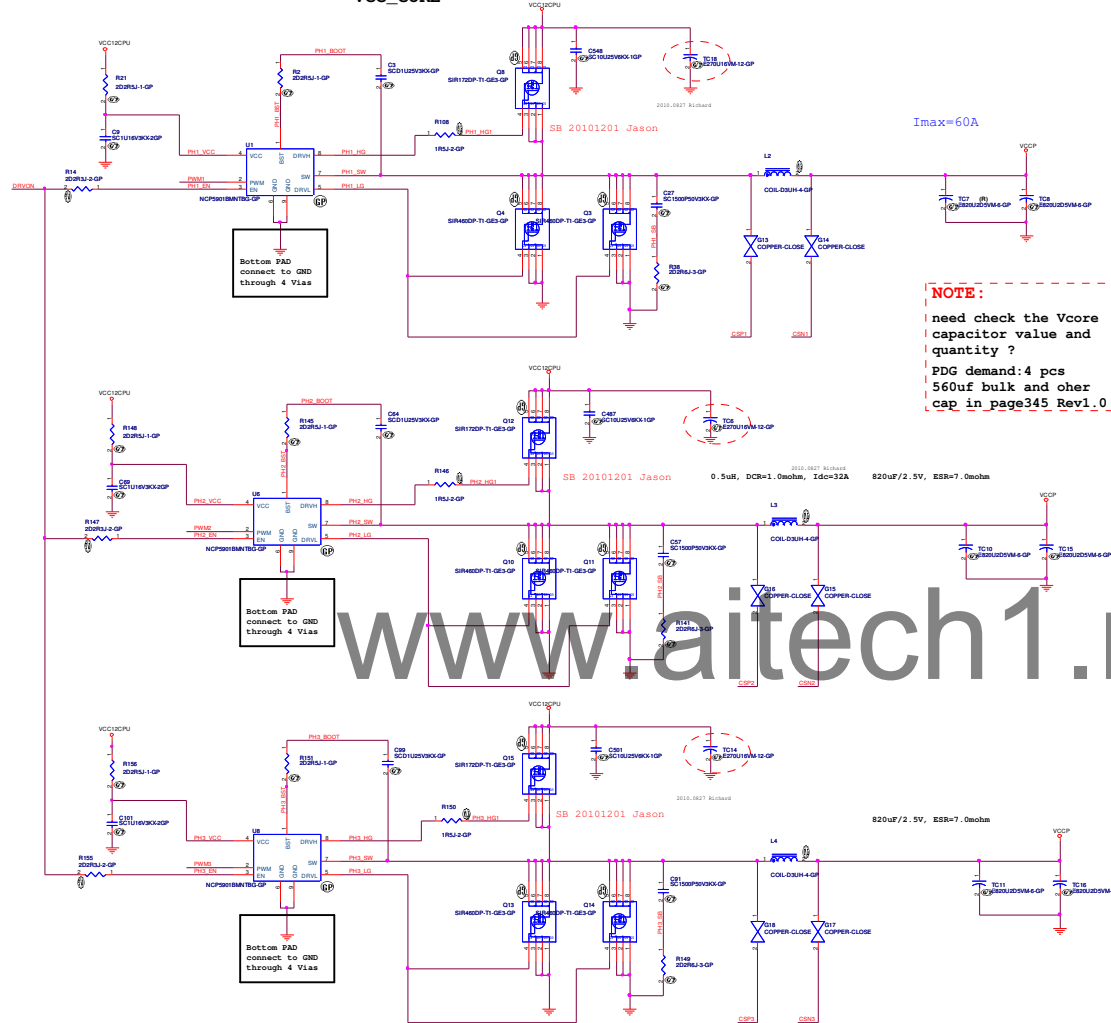


# CPU Vcore POWER

44 DRVON  
44 PWR1  
44 C5P1  
44 PWR2  
44 C5P2  
44 C5P3  
44 PWR3  
44 C5P4  
44 C5P5

VCCP Vin ripple current  $I_{max}=7A$

## VCC\_CORE



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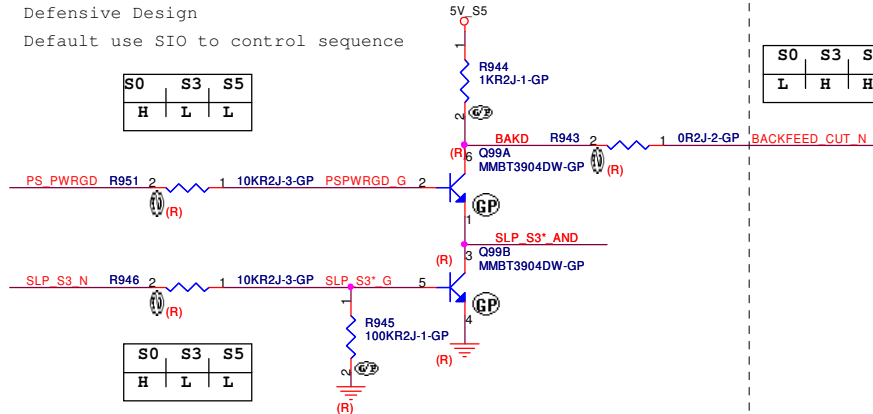
36,40 PS\_PWRGD>>  
17,24,39 SLP\_S3\_N>>  
17,24,36,37,40 SLP\_S4\_N>>  
37 BACKFEED\_CUT\_N>>

38,41,60 PC\_PWRGD <<  
37 LATCHED\_BACKFEED\_CUT <<

Defensive Design  
Default use SIO to control sequence

S0	S3	S5
H	L	L

S0	S3	S5
L	H	H

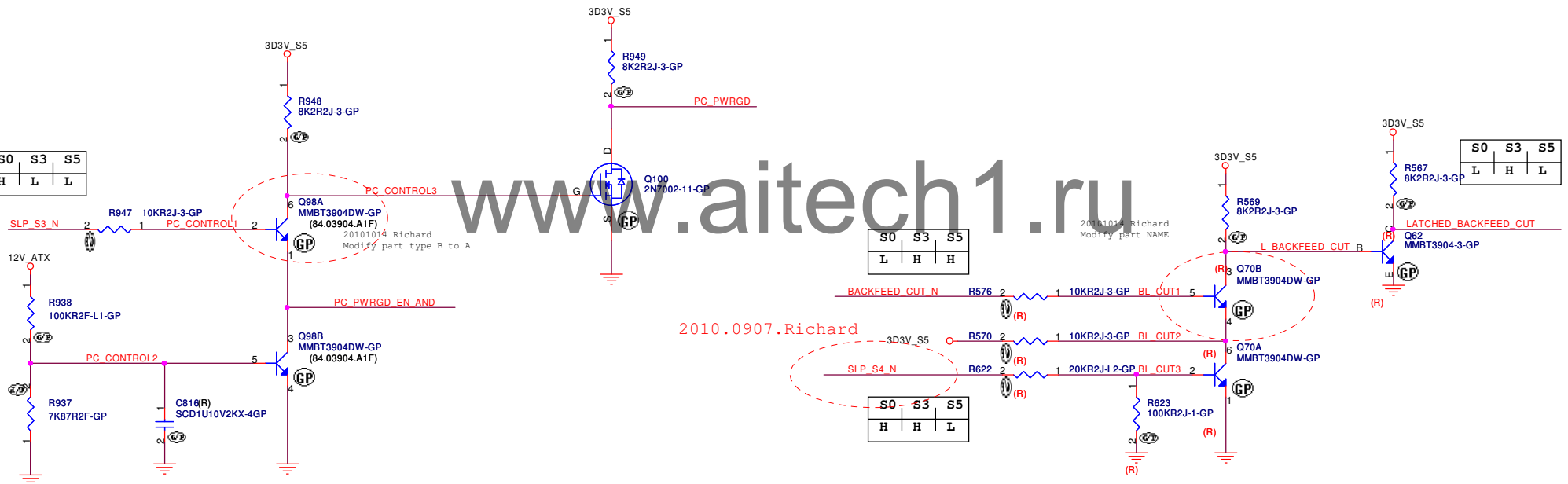


S0	S3	S5
H	L	L

S0	S3	S5
L	H	H

S0	S3	S5
L	H	L

S0	S3	S5
H	H	L



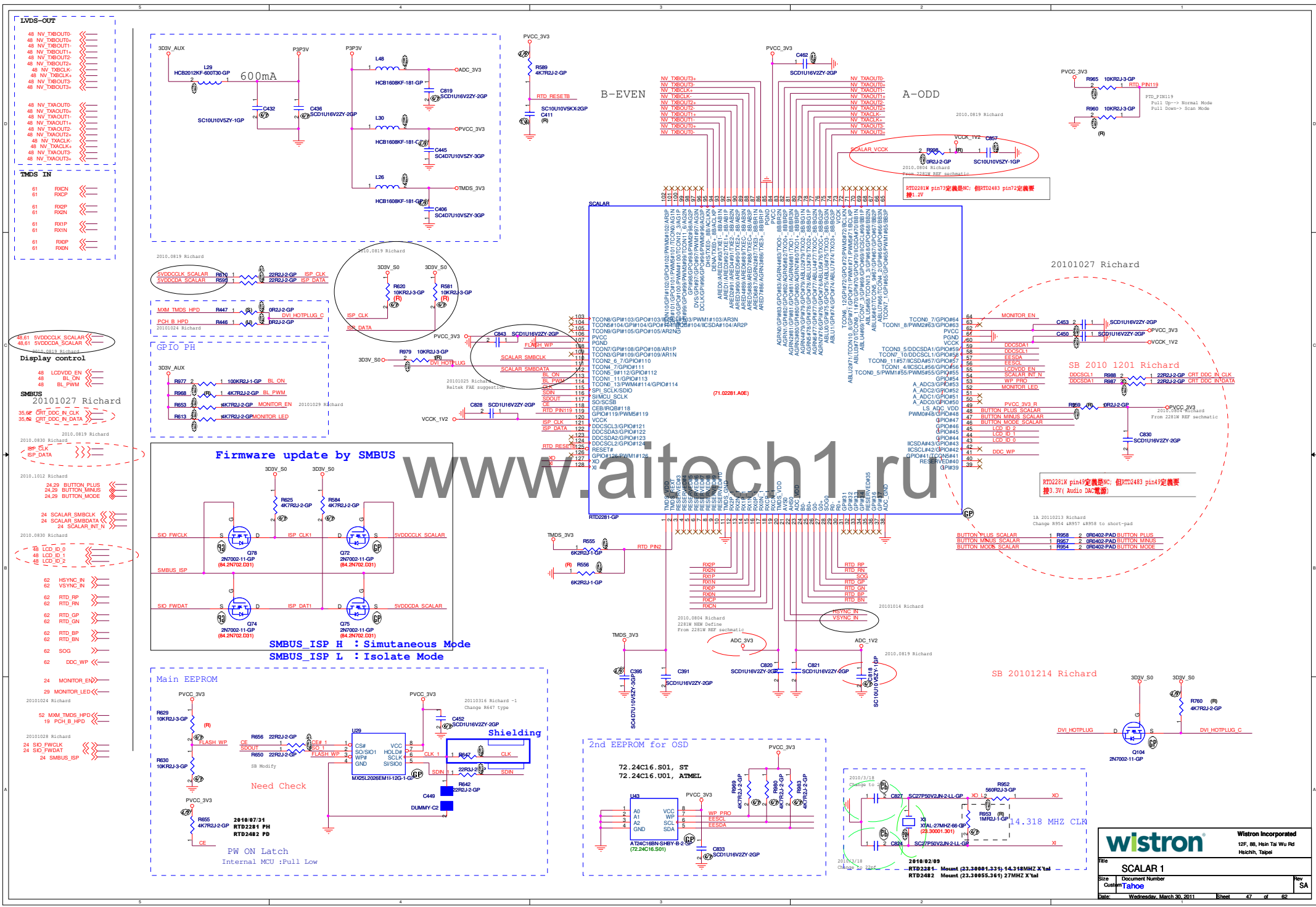
2010.0907.Richard

2010.0101 Richard  
Modify part NAME

wistron

Wistron Incorporated  
12F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title		
Size B	Document Number Tahoe	Rev SA
Date:	Wednesday, March 30, 2011	Sheet 46 of 62



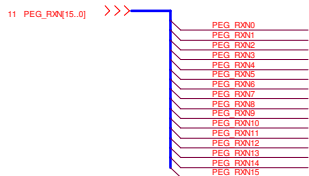
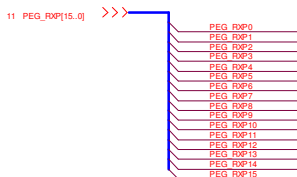
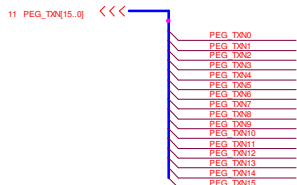
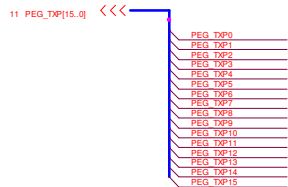




POWER REGULATORS		
+3.3V 190 mA	VDDR3	60 mA
	A2VDD	130 mA
+0.8/+1.05V	VDDC	36 A
+0.9/+1.2V	VDDCI	4 A
+1.5V 2.8A	VDDR1 +	2.8A
	DDR3 Memory	
+1.8V 1.465 A	VDD_CT	219 mA
	DP[F:A]_PVDD	20 mA
	DP[D:A]_VDD18	300 mA
	DP[F:E]_VDD18	300 mA
	SPV18	50 mA
	MPV18	150 mA
	DPLL_PVDD	75 mA
	PCIE_PVDD	40 mA
	PCIE_VDDR	440 mA
	TSVDD	
	VDDR4	5 mA
	AVDD	70 mA
	VDD1DI	45 mA
	VDD2DI	50 mA
	A2VDDQ	1.5 mA
+1.0V 1.665 A	DP[D:A]_VDD10	220 mA
	DP[F:E]_VDD10	220 mA
	SPV10	100 mA
	DPLL_VDDC	125 mA
	PCIE_VDDC	1.1 A

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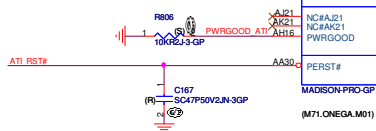
# PCI\_E x16



18 CLK\_P0E\_PEG\_N  
18 CLK\_P0E\_PEG\_P

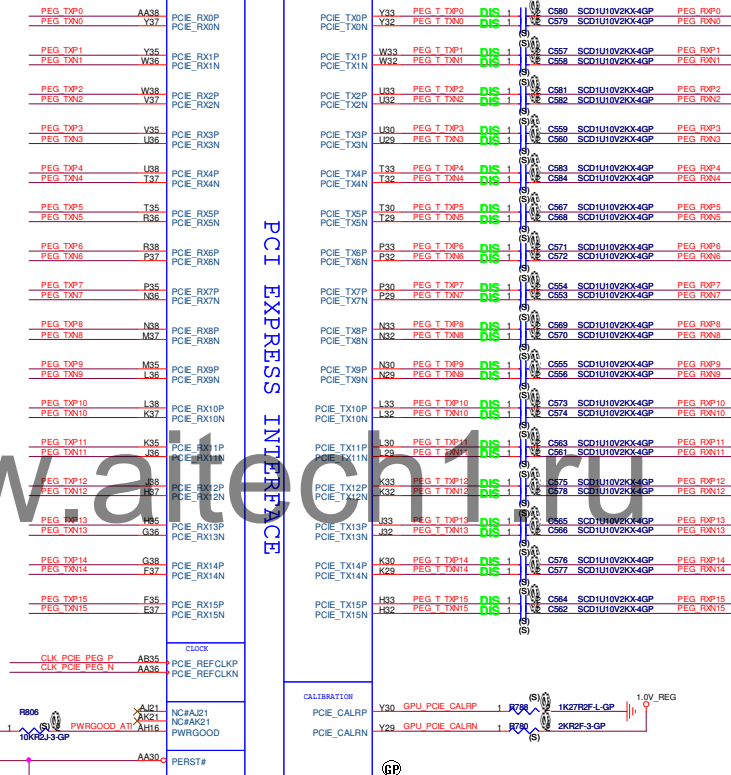
10,14,17,24 PLT\_RST\_N >>>  
R209 1 2  
URD402 PA0  
A710-SA\_0627\_CWH

SB 1202



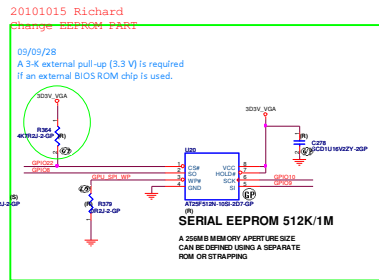
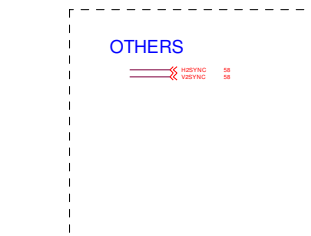
U18A 1 OF 8

## PCI EXPRESS INTERFACE



<Core Design>

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.	
File	ATI Mad PCIE
Size	Document Number
2	Tahoe
Date: Wednesday, March 30, 2011	Sheet 51 of 62



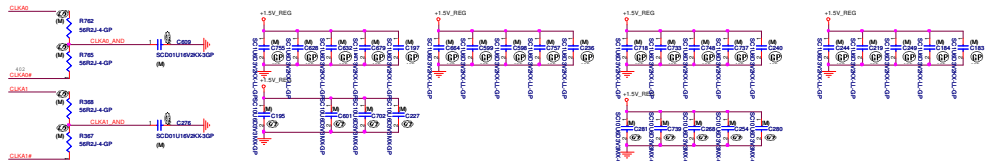
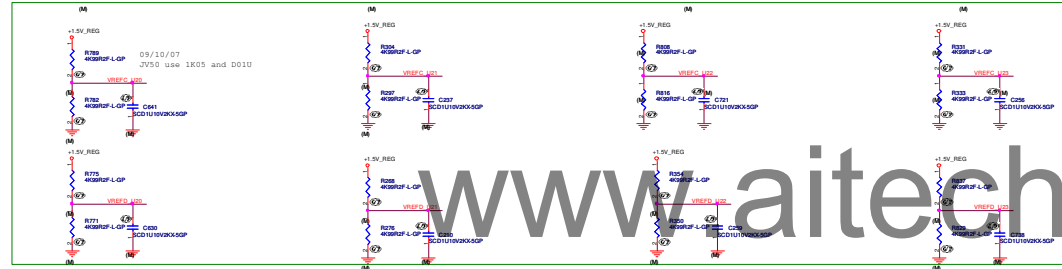
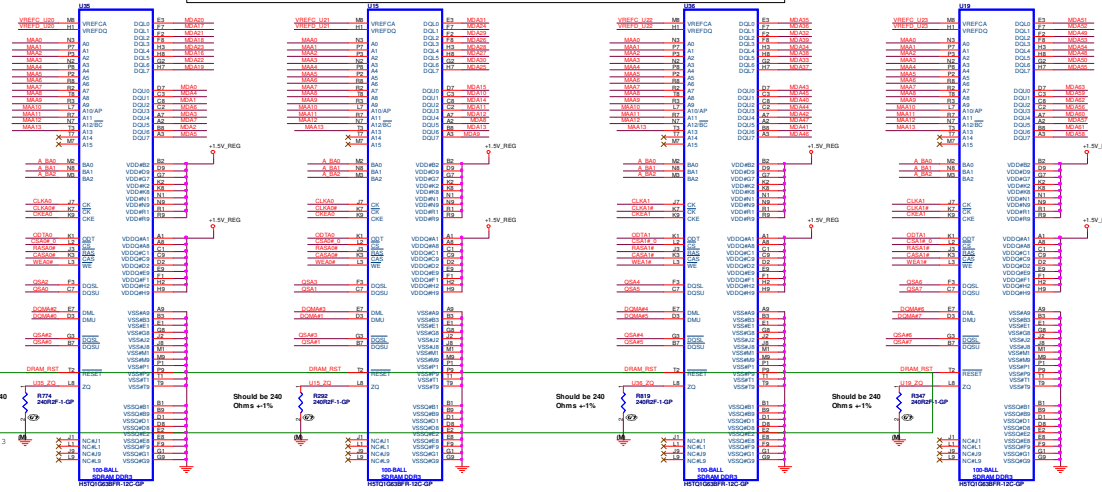






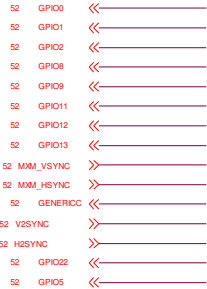
# CHANNEL A: 256MB/512MB DDR3

72.51G63.COU gDDR3 64M\*16 800MHz VRAM 54nm (Orion die) FBGA96P HYNIX H5TQ1G63BFR-12C  
72.41164.HOU gDDR3 64M\*16 800MHz VRAM E die FBGA 96P SAMSUNG K4W1G164E8-RC12

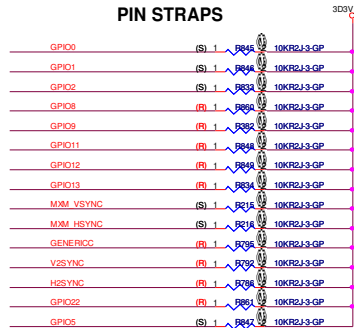


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### PIN STRAPS



3D3V\_VGA

	Manufacturer	Part Number	Size	CONFIG[2:0]
STRAP	ST Microelectronics	M25P05A	512 Kbit	100

		RESRC
STRAP	Audio for both DisplayPort and HDMI. If dongle is detected	V2SYNC

### CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,  
THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1= INSTALL 10K RESISTOR  
X= DESIGN DEPENDANT  
NA= NOT APPLICABLE

STRAPS	PN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF CLK PM EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_TX_PULL_CALIB_BP	GPIO21	BIF_TX_PULL_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG2-0	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	1 0 0
VP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNC	SMS EN HARD	0
CCBYPASS	GENERICC	CCBYPASS	0
AUD[1]	HSYNC	built-in HDMI connector	1
AUD[0]	VSYSN	Audio function present	1

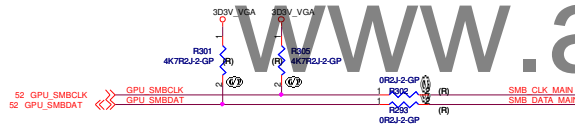
### AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,  
THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED,  
THEY MUST NOT CONFLICT DURING RESET

GPIO\_28\_TDO GPIO21\_BB\_EN



<Core Design>

For GPU Core and GPIO15/20 relationship as below:

VID1(GPIO20)	VID0(GPIO15)	Core
0	0	1.22V
0	1	1.12V
1	0	1.02V
1	1	0.92V

84.00172.037 SIR172DP  
Vgs @ 4.5V,  
Id = 13.6A,  
Rds(on) = 10.3~12.4mohm,

84.00460.037 SIR460DP  
Vgs @ 4.5V,  
Id = 10.0A,  
Rds(on) = 4.9~6.1mohm,

Vin ripple current Imax=6.04A

DCR=1.6~1.8mohm, Idc=25A

0.92V~1.22V@20A

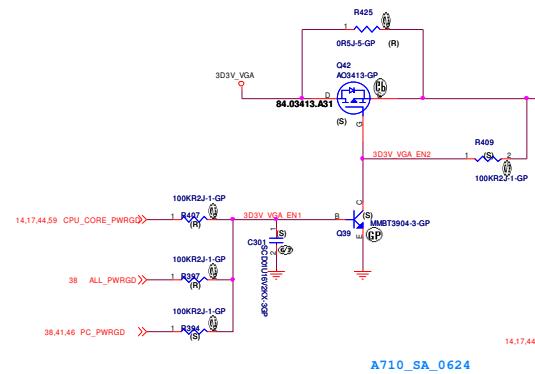
A710\_SA\_0624  
Change to DIP

820uF/2.5V, ESR=7mohm

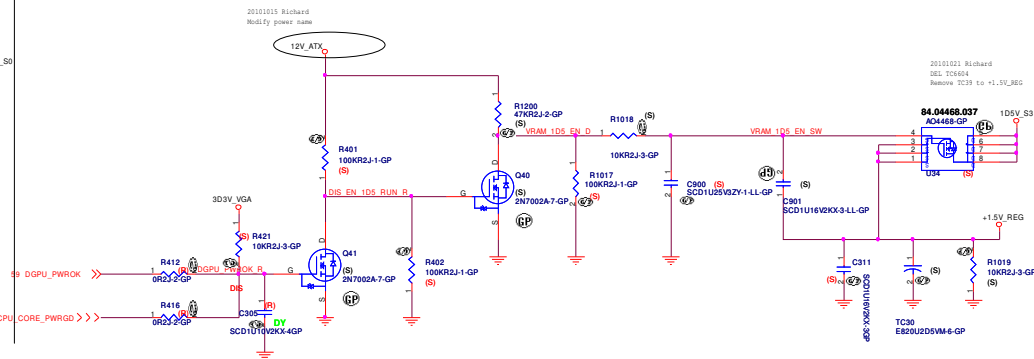
20101014 Richard

SB 20101201 Richard

### 3D3V\_S0 to 3D3V\_DELAY Transfer



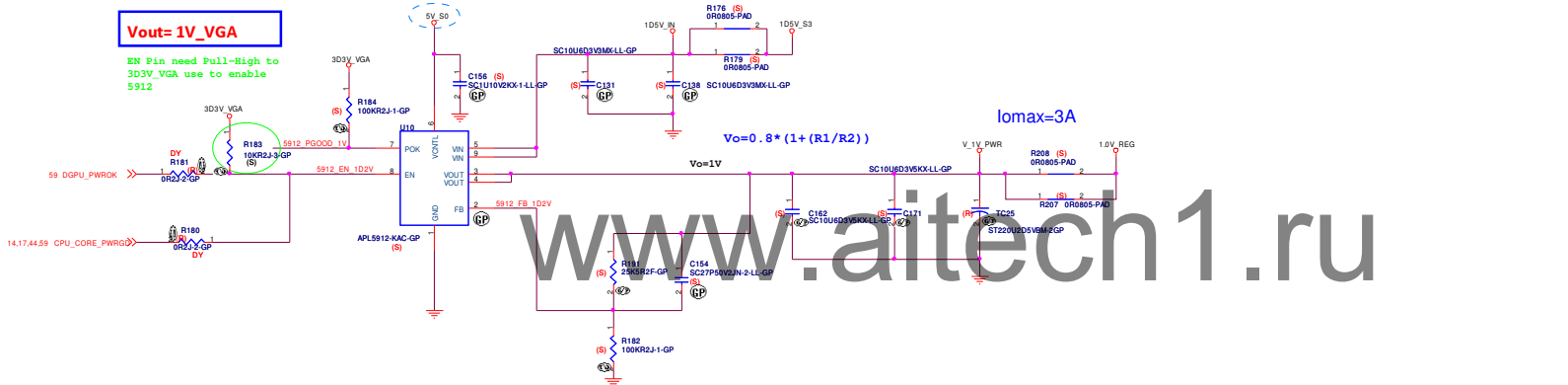
SB 20101214 Richard



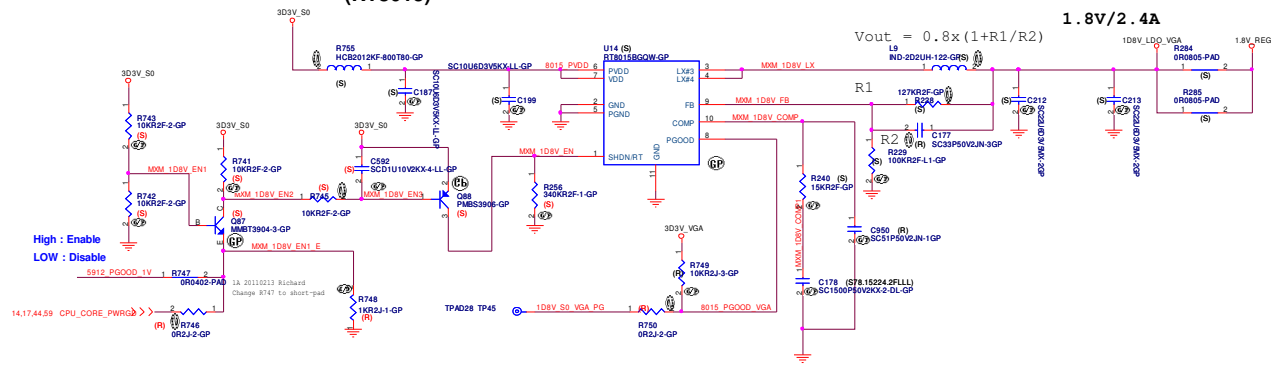
A04468, SQ-8  
Id=11.6A, Qg=9-12nC  
Rdson=17.4-22m ohm

Vout= 1V\_VGA

EN Pin need Pull-High to  
3D3V\_VGA use to enable  
5912



### 1D8V\_VGA (RT8015)



## FROM PCH DISPLAY

19 PCH\_HDMI\_DATA1+ >>>  
19 PCH\_HDMI\_DATA1- >>>  
19 PCH\_HDMI\_DATA2+ >>>  
19 PCH\_HDMI\_DATA2- >>>  
19 PCH\_HDMI\_CLK+ >>>  
19 PCH\_HDMI\_CLK- >>>  
19 PCH\_HDMI\_DATA0+ >>>  
19 PCH\_HDMI\_DATA0- >>>  
19 PCH\_D\_HPD <<<

19 PCH\_CTRL\_CLK >>>  
19 PCH\_CTRL\_DATA >>>

## FROM MXM DISPLAY

52 NV\_HDMI\_DATA1+ >>>  
52 NV\_HDMI\_DATA1- >>>  
52 NV\_HDMI\_DATA2+ >>>  
52 NV\_HDMI\_DATA2- >>>  
52 NV\_HDMI\_CLK+ >>>  
52 NV\_HDMI\_CLK- >>>  
52 NV\_HDMI\_DATA0+ >>>  
52 NV\_HDMI\_DATA0- >>>  
52 NV\_HDMI\_DETECT <<<

52 NV\_HDMI\_CLK >>>  
52 NV\_HDMI\_DATA >>>

## TO RISER

35 DDSP\_D\_TX\_DP\_0 >>>  
35 DDSP\_D\_TX\_DP\_0 >>>  
35 DDSP\_D\_TX\_DP\_1 >>>  
35 DDSP\_D\_TX\_DP\_1 >>>  
35 DDSP\_D\_TX\_DP\_2 >>>  
35 DDSP\_D\_TX\_DP\_2 >>>  
35 DDSP\_D\_TX\_DP\_3 >>>  
35 DDSP\_D\_TX\_DP\_3 >>>

35 DDSP\_CTRL\_CLK >>>  
35 DDSP\_CTRL\_DATA >>>  
35 DDSP\_D\_HPD >>>

### PCH DVI-IN

19 PCH\_TMDS\_00P >>>  
19 PCH\_TMDS\_00N >>>  
19 PCH\_TMDS\_01P >>>  
19 PCH\_TMDS\_01N >>>  
19 PCH\_TMDS\_02P >>>  
19 PCH\_TMDS\_02N >>>  
19 PCH\_TMDS\_CLKP >>>  
19 PCH\_TMDS\_CLKN >>>

### ATI DVI-IN

52 ATI\_TMDS\_00P >>>  
52 ATI\_TMDS\_00N >>>  
52 ATI\_TMDS\_01P >>>  
52 ATI\_TMDS\_01N >>>  
52 ATI\_TMDS\_02P >>>  
52 ATI\_TMDS\_02N >>>  
52 ATI\_TMDS\_CLKP >>>  
52 ATI\_TMDS\_CLKN >>>

### TMDS OUT

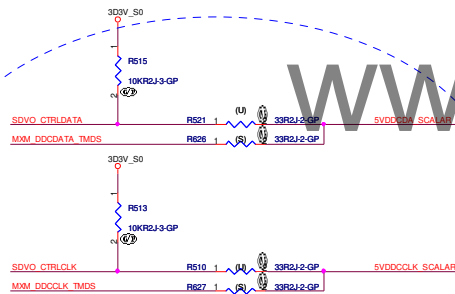
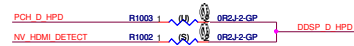
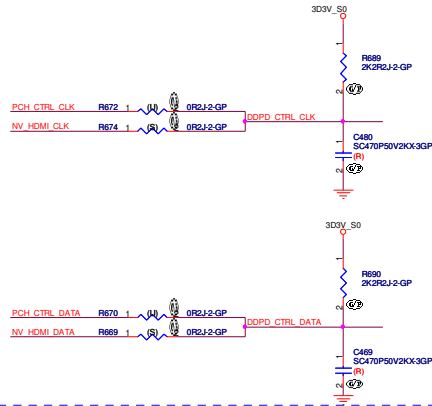
47 RXCN >>>  
47 RXCP >>>  
47 RX2P >>>  
47 RXCN >>>  
47 RX1P >>>  
47 RX1N >>>  
47 RX2P >>>  
47 RXCN >>>

19 SDVO\_CTRLDATA >>>  
19 SDVO\_CTRLCLK >>>

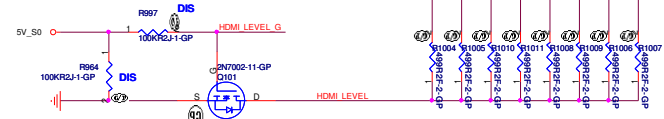
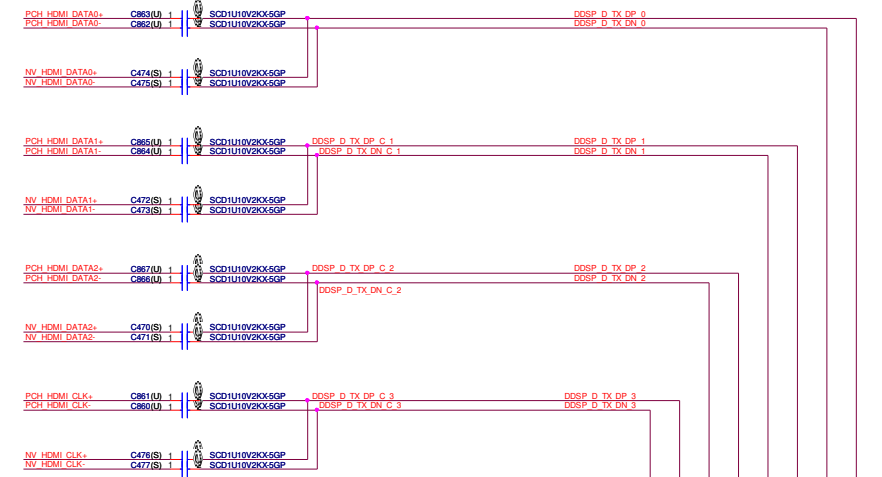
52 MXM\_DDCDATA\_TMDS >>>  
52 MXM\_DDCCLK\_TMDS >>>

47,48 SVDDCA\_SCALAR >>>  
47,48 SVDDCLK\_SCALAR >>>

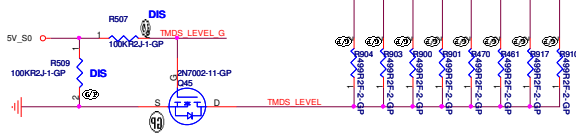
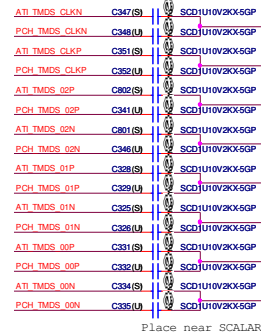
## HDMI



20101028 Richard  
PCB DVI LEVEL SHIFT & AC CAP  
Combine with HDM SB 20101201 Richard



20101028 Richard  
PCB DVI LEVEL SHIFT & AC CAP  
Combine with HDM SB 20101201 Richard





47	RTD_RP	
47	RTD_RN	
47	RTD_GP	
47	RTD_GN	
47	RTD_BP	
47	RTD_BN	

